Next Generation On-Board Sensor Technologies for Rolling Stock

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16. Abstract.

Previous research and commercial pilot tests have demonstrated that wireless onboard bearing and wheel monitoring have significant advantages in detecting and predicting defect conditions, including improved sensitivity, accuracy, and early-stage warnings that enable preventive maintenance. The project described in this report aims to produce a compact, modular, and flexible onboard system specifically designed to enable research into techniques such as: (a) improved sampling rates and processing, (b) data fusion from multiple bearings to improve accuracy and detect more types of hazards, (c) more efficient communication protocols leading to extended battery life, and (d) comparison of multiple energy harvesting methods. In this project phase, the primary focus was development of hardware, leading to a design that is small (64mm × 32mm × 20mm, exclusive of battery), with interchangeable modules for communications using different frequency bands and formats, as well as improved resolution, memory, and computation capacity compared to earlier devices.

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Table of Contents

List of Figures

List of Tables

List of Abbreviations

ABD	Acoustic Bearing Detector
ADC	Analog-to-Digital Converter
BLE	Bluetooth Low Energy
BPSK	Binary Phase Shift Keying
CMRR	Common Mode Rejection Ratio
DAQ	Data Acquisition
FCC	Federal Communications Commission
FFT	Fast Fourier Transform
FSK	Frequency Shift Keying
GPIO	General Purpose Input/Output (microcontroller pins)
HBD	Hot Bearing Detector
HF	High Frequency
I^2C	Inter-Integrated Circuit (bus)
ISM	Industrial, Scientific and Medical (frequency band)
JTAG	Joint Test Action Group (programming and debug standard)
LDO	Low Drop Out
LF	Low Frequency
LPF	Low Pass Filter
MEMS	Micro-Electromechanical System
MPPT	Maximum Power Point Tracking
MSK	Minimum Shift Keying
PCB	Printed Circuit Board
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RF	Radio Frequency
RMS	Room-Mean-Square
RSSI	Received Signal Strength Indication
RTOS	Real Time Operating System
RTD	Resistance Temperature Detector
SAR	Successive Approximation Register (analog-to-digital conversion)

SPI	Serial Peripheral Interface (bus)
SRAM	Static Random Access Memory
SWD	Serial Wire Debug (programming and debug standard)
TEG	Thermoelectric Generator
USDOT	U.S. Department of Transportation
UART	Universal Asynchronous Receiver Transmitter
UTCRS	University Transportation Center for Railway Safety

Disclaimer

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1 Introduction

1.1 Background

Derailments due to wheel, bearing, or track defects can lead to hazardous chemical spills, service stoppages and costly interruptions, and, most importantly, may result in fatalities. Even failures that are identified prior to causing a derailment have economic impact due to routes blocked for field repairs. Systems based on wayside detection or human inspection do not provide continuous monitoring and typically only detect impending failure. Previous research [1-5] has indicated that wireless vibration sensors mounted on railroad suspension components (see Figure 1) can effectively predict the need for bearing replacement tens of thousands of miles in advance of impending failure. Sensors of this type are now undergoing limited field implementation [6-7] and have shown an additional ability to identify wheel and track defects [8]. Addition of further sensing modalities in the same system (temperature, bearing load [9], and location awareness) has the potential for early detection of a wide variety of hazardous situations.

1.2 Project Objectives

Previous work focused on individual, autonomous sensors that spontaneously detected problems through a network to a central hub. With widespread deployment on multiple bearings throughout a train, a new opportunity arises to fuse data from multiple sensors to (a) detect and identify entire new classes of hazard, and (b) improve accuracy for classes of hazard that are already detectable. Examples of the possible use of data from multiple sensors to improve accuracy and to isolate sources of impact are summarized in Section 2.

This opportunity depends on having access to multiple sensors with precision synchronization of data collection (perhaps ten microseconds or better) and accurate system awareness of sensor position (within a few centimeters). The long-term aim of this project is to build a deployment-ready system capable of making and then analyzing such measurements. For the 15-month project reported here, the goals were to design and build the required electronics and embedded software, while laying foundations for machine-learning based analysis of the field data to be obtained in future phases of the project. Section 3 covers the system architecture at the block diagram level. Sections 4, 5, and 6 cover each of the main function blocks in more detail. Section 7 describes an

alternative onboard but wired system that has higher data throughput capability and can be used for data collection to validate sensor fusion concepts.

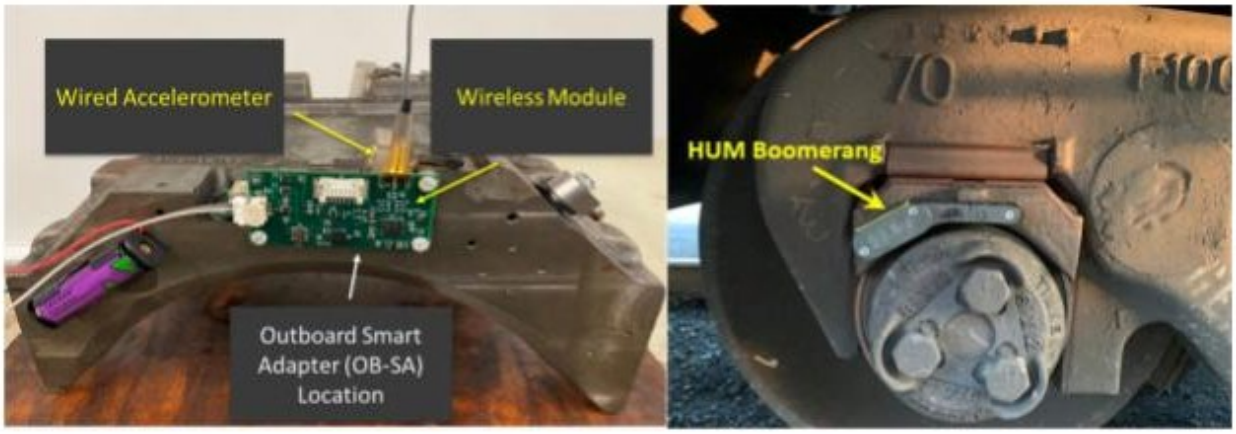

Figure 1: Railcar bearing adapters with mounted sensors [7]

(Left) Earlier generation UTCRS wireless sensor, mounted on an adapter in the lab. (Right) Hum Industrial Technologies, Inc., wireless sensor installed in field service.)

1.3 Usage Disclaimer

The system described in this report is intended for use as a testbed for research into onboard sensing. It is not intended, nor is it suitable for commercial deployment or usage in regular railroad service. Among other limitations, (a) the electronic components used do not necessarily meet temperature range requirements for rail service, (b) the packaging and connectors are not suited for long-term all-weather service, and (c) the digital and communication portions, while designed with what the authors consider to be general good practice for electromagnetic compatibility, have not been tested or certified for FCC Part 15 compliance.

2 Motivation and Requirements

An earlier generation of UTCRS wireless sensor is shown in Figure 1. More information on this sensor is available online at http://railwaysafety.utrgv.edu/. While this device was successful in demonstrating the feasibility of wireless onboard bearing monitoring, its design had several restrictions that limited opportunities for future research and field deployment.

- The only wireless protocol supported was Bluetooth Low Energy (BLE). This places hard limits on range and data rate and does not allow for comparative radio propagation studies of different frequency bands in a railroad environment.
- The microcontroller used a real time operating system (RTOS) that made timing more complicated and occupied large amounts of static random-access memory (SRAM). This, in turn, limited the number of vibration waveform samples that could be taken in one sequence (a "shot"), and limited the amount of workspace for signal post-processing.
- It used a low resolution (12-bit) analog-to-digital converter (ADC) that limits the dynamic range of measurements.
- Because communications were through BLE and were mediated by the RTOS, the start times of data collection shots among multiple sensors could not easily be synchronized to closer than ~10 milliseconds.

While all four of these restrictions are important to overcome to improve the flexibility, range, and performance of the sensors, overcoming the last restriction opens up new avenues for research in joint processing of vibration waveforms from multiple sensors.

Figure 2 summarizes some potential advantages of joint processing. It is known from prior laboratory testing at UTCRS that there is some level of crosstalk between bearings on a single axle. An undamaged bearing immediately adjacent to a damaged bearing on the same test rig will show a rise in RMS vibration level that tracks, but is less than, the RMS of the damaged bearing. Typical values would be 5g RMS measured at the undamaged bearing due to 15g RMS generated by the damaged bearing. The crosstalk will be much lower in field service with a full-length axle, nevertheless, removal could improve accuracy in detecting small defects.

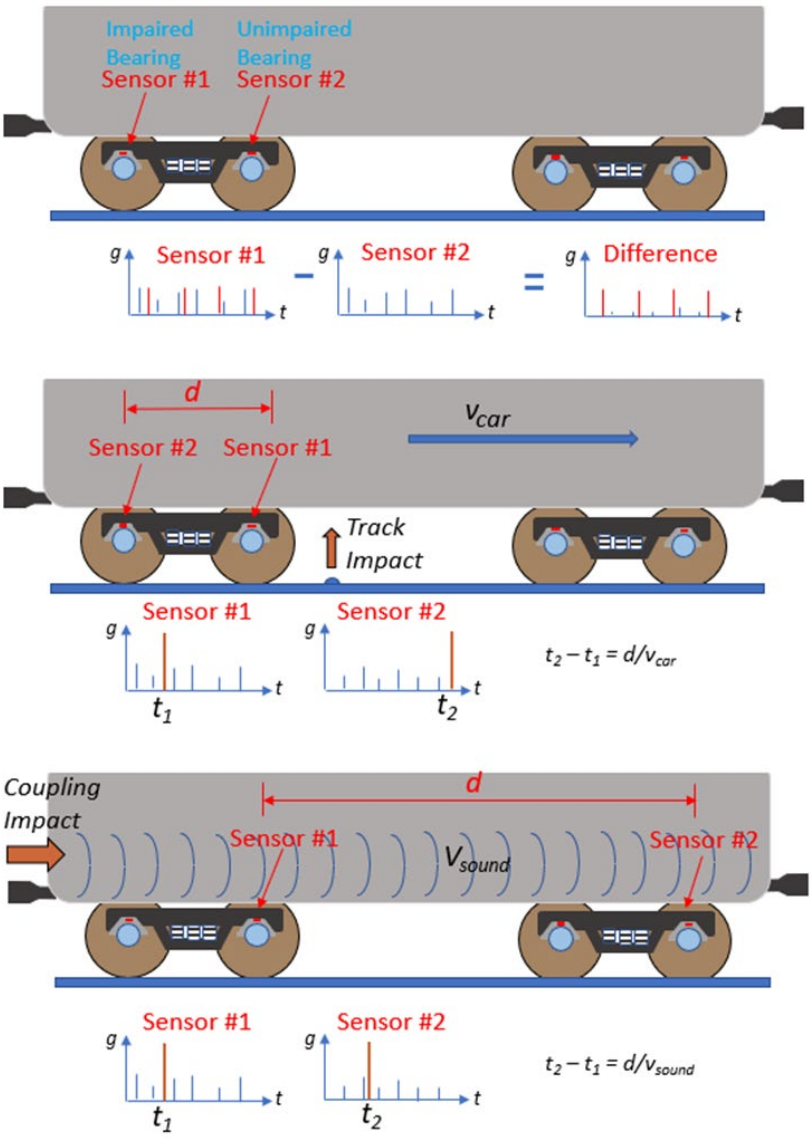

Figure 2: Advantages of synchronized sampling in multiple sensors

(Top) Comparison of signatures from two bearings on the same side frame can be used to partially cancel noise sources originating in other parts of the railcar. (Middle, Bottom) Sources of single impact events can be distinguished through differential timing combined with sensor position awareness.

A second potential benefit is identifying the source of single impact events. Bad track segments and impacts due to over-speed coupling both cause single spikes in acceleration at each sensor. Using current methodology, these single event impacts are easily distinguished from bearing and wheel defects since they are not periodic; however, the two types of single event impacts are not

easily distinguished from each other. As shown in Figure 2, *synchronized* data from two sensors at different known locations on the railcar should aid in determining the source of impacts.

The objective of this project is to produce a next-generation device that enables synchronized sampling, overcomes the other restrictions of earlier devices, and provides flexibility for further research in communications, energy harvesting, and integration of other sensors. Table 1 shows the target requirements for the new design.

Table 1: Wireless Sensor Module Requirements

Category	Requirement
a. Power Source	Initial design should be able to operate from any of the following (1) a primary battery, (2) single or dual thermoelectric generators (TEGs), or (3) solar cells. In addition, the system should have reasonable flexibility to accommodate energy harvesting sources not yet contemplated without a complete redesign.
b. Energy Storage	Should be able to operate (1) using no energy storage other than the primary battery, or (2) using supercapacitor storage, or (3) using a rechargeable lithium battery.
c. Power Distribution and Management	(1) All sensors and peripherals outside the primary MCU should be able to power down separately, with an inactive current of less than 2µA each. (2) All devices except those related to energy harvesting and battery/supercapacitor management should operate at 3.3V or less.
d. Sensor - Vibration	Design should include a high-performance analog accelerometer with (a) dynamic range to capture impacts at least up to 50g, (b) mechanical bandwidth of 5 kHz or better, and (c) noise floor sufficient to measure RMS with 0.1g repeatability. In the case of an analog accelerometer, sharp-cutoff analog low-pass filter is required after the accelerometer but prior to analog-to-digital conversion. It should have the following features: (d) adjustable filter cutoff frequency from (at least) 500 Hz to 5kHz. Preferably this cutoff is under firmware control; however, this feature may be reserved for future versions. See Section 4. (e) stopband rejection >60dB (f) stopband starting no higher than 1.2 times the cutoff frequency.

	(g) can be bypassed under firmware control. In the case of a digital accelerometer options for sample rates to at least 25 kHz are needed to allow for flexibility in digital filtering in firmware.
e. Sensor – Temperature	Design should include a temperate sensor within the module capable of ±2ºC accuracy over at least -50ºC to 125ºC. Preferably the sensor itself should be able to measure to 200ºC assuming other portions of the electronics are still functional.
f. Sensors - Load	Design should include support (power, signal conditioning, and temperature monitoring) for a strain-gauge based load sensor outside the module.
g. Primary Microcontroller	The primary MCU should have (1) ability to maintain a background timer accurate to better than 10ppm and monitor wakeup pins while consuming less than 50µA of current, (2) when running at full speed, current consumption close to the best available, preferably less than 100µA/MHz. (3) data paths at least 16 bits wide and the ability to efficiently handle 32-bit calculations. (4) sufficient *free* on-chip RAM to store at least 16,384 samples of 16 bits each and perform at least a 16,384-point FFT with 16-bit accuracy for the real and imaginary parts. (5) serial communications via SPI and I^2C to at least 1 MHz clock rate, and UART to at least 115 kbaud. Preferably any of the three protocols can be mapped to the same set of physical I/O pins in firmware. (6) at least four independent timer/counter units to support multiple timed processes running simultaneously. (7) general purpose ADC conversion (4 channels or more) for non-critical measurements. 12-bit resolution and 100kHz sample rate is sufficient. Note that the primary ADC for vibration and load needs higher performance described below and can be a separate unit. (8) a PWM modulation unit capable of generating waveforms up to at least 500kHz. Duty cycle control does not need to be accurate or have high resolution; the PWM may be used to clock the accelerometer filter. (9) suitability for bare-metal programming without the use of a real-time operating system, closed-source libraries, or licensed firmware, if required by the application.
h. Analog-Digital Conversion	(1) At least four channels of ADC conversion should be available with at least 16-bit resolution. It should be possible to sample, convert, and serially read any channel in less than 50µs; faster performance is preferred.

	(2) Consistent with requirement (1), the ADC should be low power, preferably less than 1mA while active. Like all other peripherals, ADC should have a shutdown current of less than 2μA.
i. Wireless Communication Standards	The initial module hardware should be able to support any of the following, possibly by swapping hardware modules: (1) LoRa in the 902-928 MHz ISM band. (2) Generic FSK in the 902-928 MHz ISM band. (3) Bluetooth Low Energy in the 2.4-2.48 GHz ISM band. (4) Generic IEEE 802.15 in the 2.4-2.48 GHz band. (5) Ability to implement mist^{TM} with appropriate proprietary firmware and upgraded timing components. (6) Reasonable flexibility to implement other standards not yet contemplated without a complete redesign.
j. Wireless Communications – Other Requirements	(1) At least the 902-928 MHz hardware should be able to generate a hardware interrupt upon completed reception of a packet, with interrupt latency strictly consistent to better than 10μs. (2) All hardware should be designed to be capable of complying with FCC Part 15 standards for power output, out-of-band spurious emissions, frequency hopping, and bandwidth. (3) Each receiver should be capable of providing RSSI information, preferably to a resolution of ±1dBm or better. (4) External (off-board) antenna. (5) Each module should be able to go into sleep mode with less than 2μA consumption, if requested by the primary MCU via a serial control line (one of the following: SPI, I^2C, or UART).
k. Physical Dimensions	Less than 3×1.5×1 inches (75×38×25 mm) exclusive of antenna and battery.
l. Temperature Range	Final design should use components rated for at least -40ºC to +125ºC. (Preliminary versions for alpha testing may use some commercial range (0ºC to 70ºC) components.)
m. Structural Requirements	(1) The accelerometer should be mounted in a portion of the module rigidly clamped to the bearing adapter to ensure proper transmission of vibration. If the board is positioned off the adapter surface, the accelerometer should be placed between two pinned locations (mounting screws or pins) rather than at the end of any cantilevered section. (2) Conversely, the battery (or other large masses) should not be mounted on or rigidly connected to the same PCB on which accelerometer is mounted.

3 Modular Concept for On-Board Sensing Testbed

To meet the requirements in Table 1, a modular system is proposed as shown in Figure 3. The three separate shaded areas represent separate connectorized modules. The rationale for this choice of division is as follows: The primary microcontroller (MCU) and sensors (vibration, temperature, and load) have a large number of interconnections, and the signal paths need to be low noise. Furthermore, redesign of one of the sensors or its signal conditioning will likely require hardware modifications to the MCU wiring. Therefore, all are placed in one module.

On the other hand, the connection between the battery management and the MCU is relatively uncomplicated and can be easily standardized. Placing the battery management on a separate daughterboard allows exploration of different energy harvesting methods and evaluation of different storage devices, without hardware modifications to the main board.

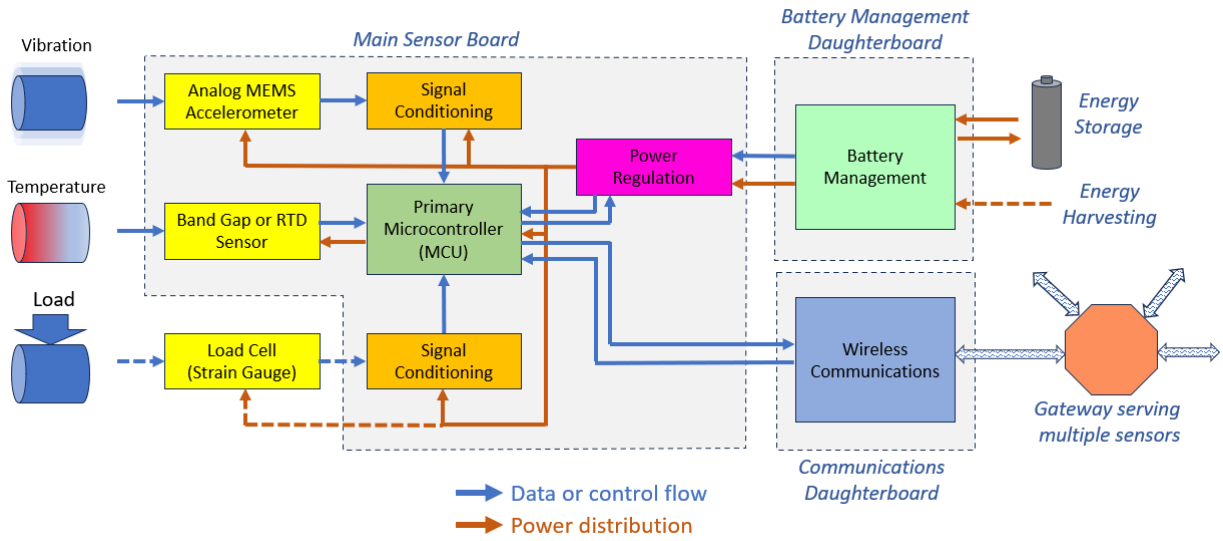

Figure 3: Block diagram of next generation onboard testbed

One active area of future research will be communications protocols and wireless propagation characteristics over railcar-to-locomotive and railcar-to-wayside paths, for different frequency bands and signal bandwidths. For this reason, the communication hardware is also placed on a separate daughterboard, with a serial interface to the mainboard. The serial interface can be reconfigured in firmware to use SPI, I2C, or UART protocols as needed. The connector also includes a pin that allows the communications module to issue a hardware interrupt direct to the MCU. This provides the possibility of closely synchronizing the start of a data acquisition shot to

the receipt of a "start now" packet broadcast from a gateway to multiple onboard sensors, with timing errors limited primarily by the speed of radio wave propagation, or about 60-70ns over the length of a railcar.

A conceptual diagram of the physical layout is shown in Figure 4. The main sensor board has the accelerometer onboard and will be mounted rigidly to the outboard face of the bearing adapter to ensure tight coupling for transmission of vibrations. The two daughterboards will each be attached by a connector plus two standoff mounting screws.

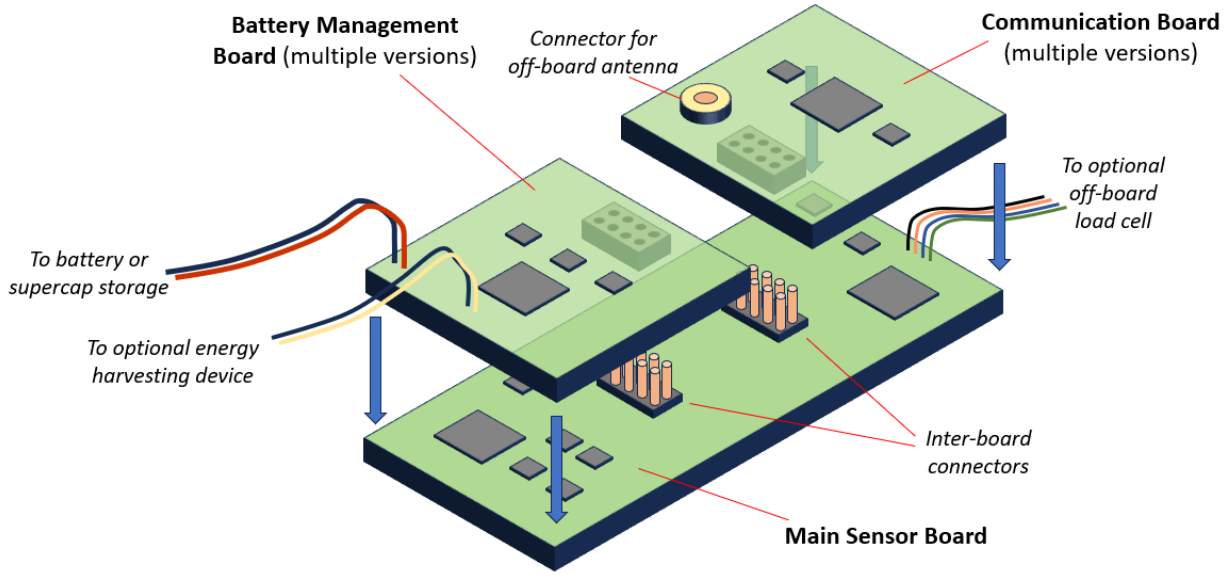

Figure 4: Conceptual diagram of modular assembly

Vertically exploded view. Target assembled size is 2.5in ×1.25in×0.4in (63.5mm×31.8mm×10.1mm)

The following sections of the report will describe the main sensor board, two separate designs for the communications daughterboard, and two separate designs for the battery management daughterboard.

4 Main Sensor Board

4.1 Overview

The Main Sensor Board includes the primary MCU, the accelerometer and (if required) associated low-pass filter, two options for temperature sensors, conditioning for signals received from an off-board load sensor, and power enable/disable controls. Three different versions of the main sensor have been designed, with the same MCU and external interfaces, but with different accelerometers and signal processing chains. Versions 1 and 2 employed an analog output accelerometer and an analog filter prior to analog-to-digital conversion; Version 3 uses a single-chip accelerometer with onboard conversion and digital output.

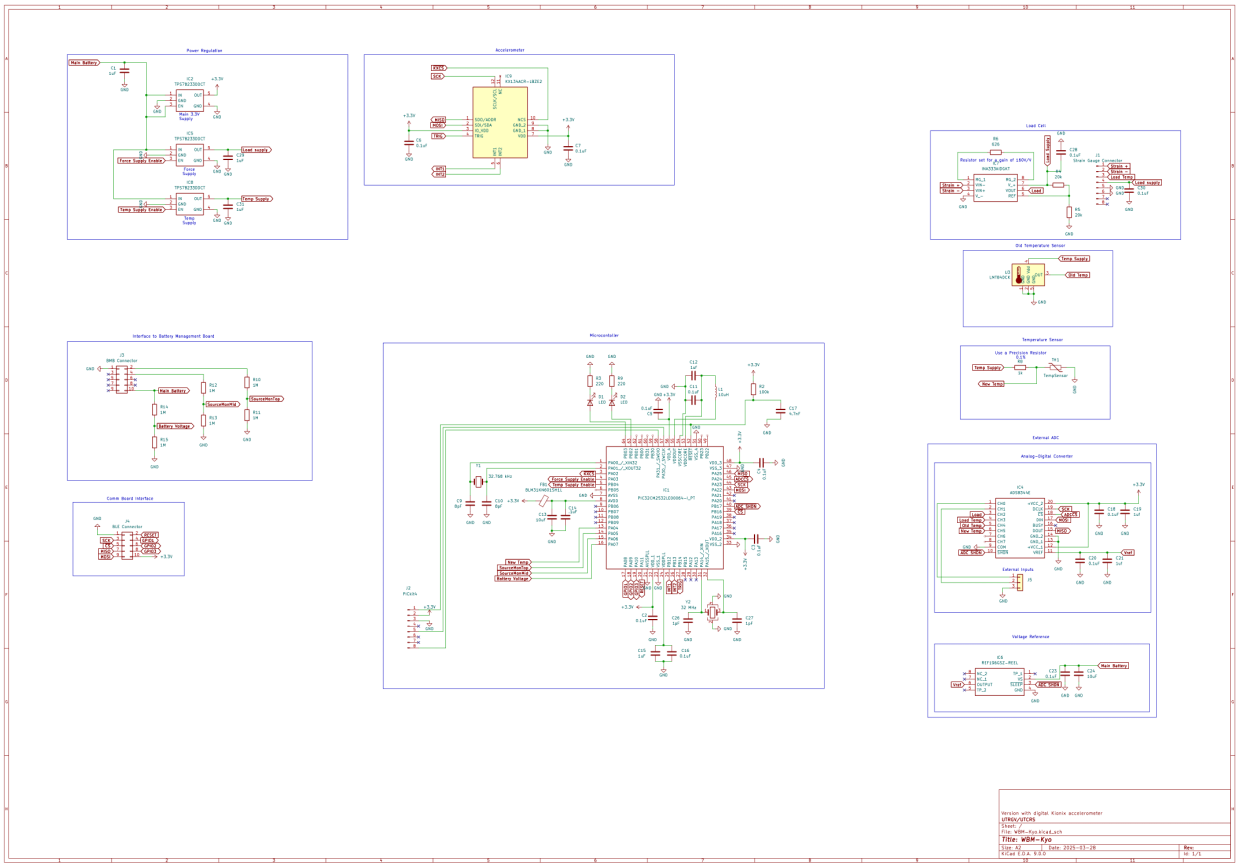

Figure 5: Schematic of main sensor board

(Version 3 Schematic. Note: This high-resolution image can be zoomed to view more detail)

Versions 1 and 2 contain circuitry similar to a proprietary design, so they will not be presented in detail here. The schematic for Version 3 is shown in Figure 5 below. Each major subsection is discussed in further detail below.

4.2 MCU Circuitry

The microcontroller is a PIC32CM3532LE00064 produced by Microchip. It was selected primarily for the following features:

- Very low power consumption (<15 μA/MHz when active, and 1.7mA for standby with SRAM contents preserved).
- Large onboard RAM (512kB). The MCU easily meets the Table 1 requirement of memory to perform a 16,384-point FFT, which is required for the UTCRS Level 2 algorithm.
- Sufficient number (80) of GPIO pins.
- Flexible assignment of internal peripherals to GPIO pins.

The support circuitry around the PIC32CM3532LE00064 MCU is shown in more detail in Figure 6. The MCU has internal clocks available; however, their accuracy does not meet requirements for sample rate and wake-up time accuracy. Therefore, the external crystal options are used with two separate oscillators. One high frequency (HF) oscillator runs at 32 MHz and serves as the primary clock when the MCU is awake. It is shut down during sleep mode to conserve power. All of the following are derived from the HF oscillator either directly or indirectly:

- Instruction rate
- Accelerometer sample rate
- Clocks for SPI and onboard 12-bit ADCs

The second low frequency (LF) oscillator runs at 32.768KHz. Currently, the plan is to operate the LF oscillator continuously regardless of sleep/wake status, to clock a counter that provides a time reference for wake-up events, either periodic when operating autonomously or after a timed-sleep instruction received from the gateway. It will also be used to time communication windows.

The crystal selected for the LF oscillator has ±5ppm accuracy, which translates to ±432 milliseconds per day drift. In a network which saves power by using very tight communication windows, it will be important to correct for the drift. This will be accomplished by resetting the counter when specified timing packets are sent from the gateway, which in turn will typically have

a GPS-corrected real time clock. For most of the experiments planned for this system, highly accurate real time is not needed but precise alignment between the gateway time and sensor module time is an absolute requirement.

Connector J2 in the lower left of Figure 6 is the programming connector; it is only used to flash firmware onto the MCU and is neither used nor accessible when the daughterboards are installed.

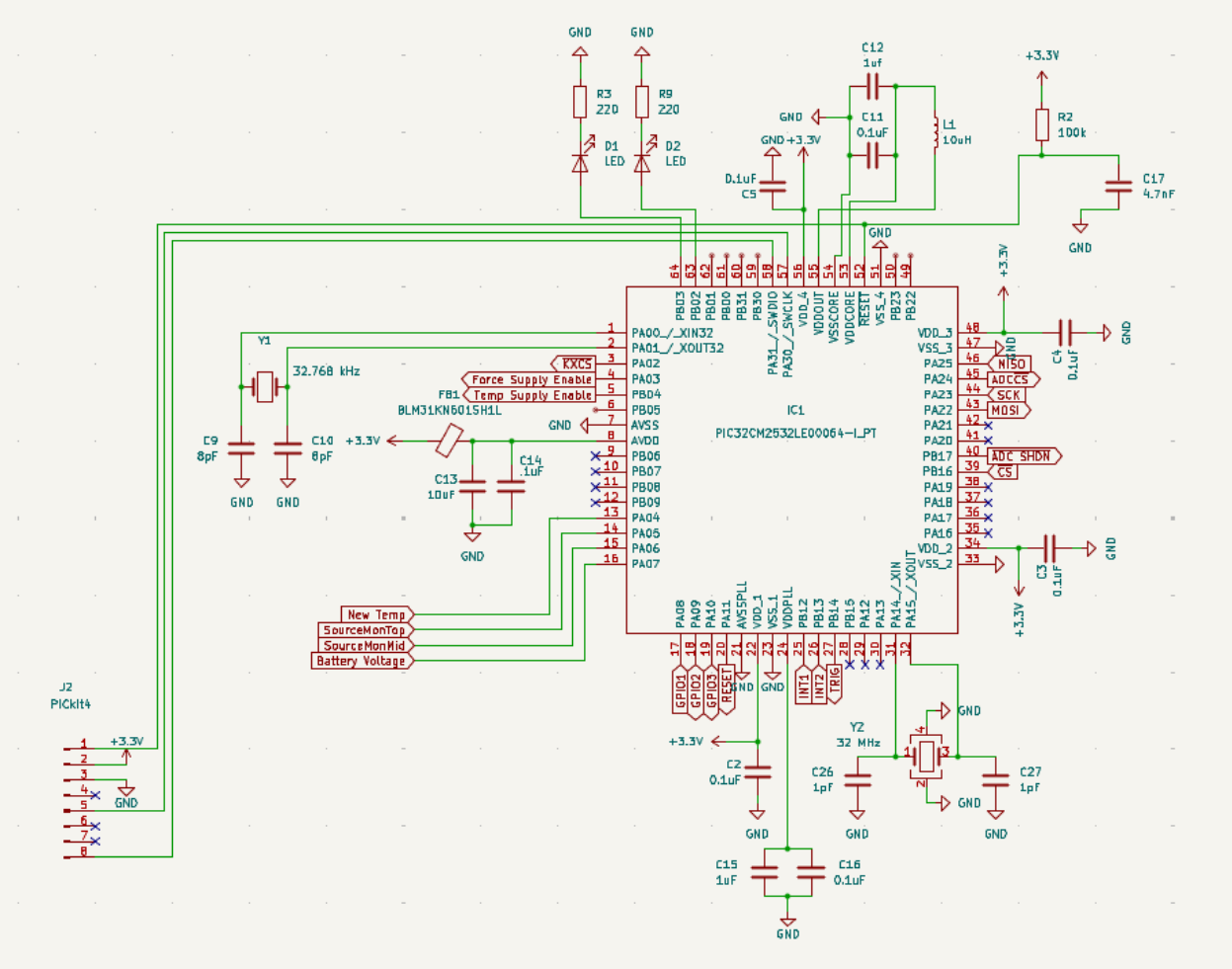

Figure 6: Main sensor board detail: MCU

(Version 3)

4.3 Power Regulation

The power regulation circuitry is shown in Figure 7. All devices on the main board operate using 3.3V supplies. Standard LDO regulators are used with separate regulators for the temperature sensors and load conditioning. The regulators can be enabled or disabled independently by the

MCU except for the one (IC2) powering the MCU itself. The MCU will manage its own sleep/active times via firmware control.

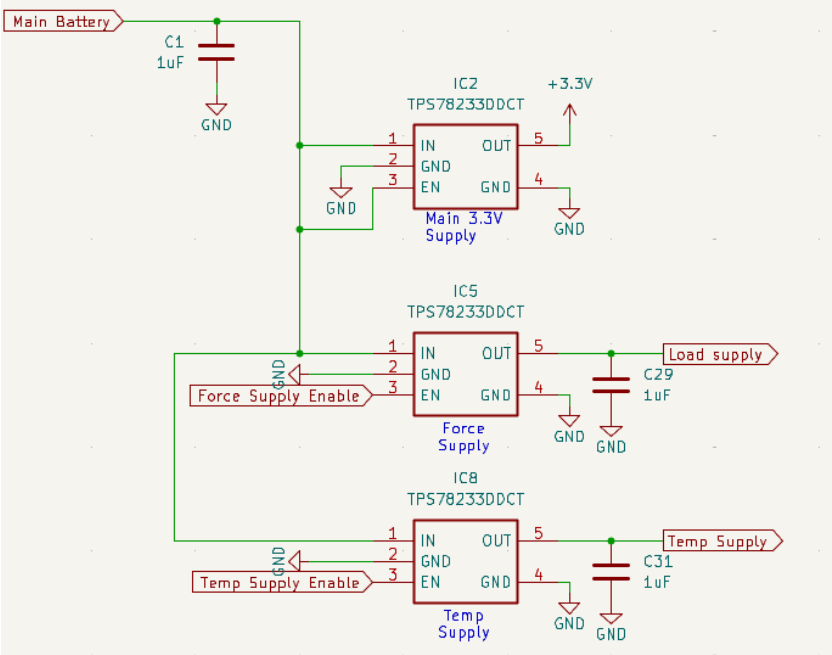

Figure 7: Main sensor board detail: Power regulation

(Version 3)

4.4 Digital Accelerometer

As stated above, different accelerometers and signal conditioning strings are used in different versions. Version 3 uses no proprietary circuits or settings and is presented here in Figure 9. IC9 is a Rohm Semiconductor Kionix® series three-axis, digital output accelerometer, part number KX134ACR-LBZE2. It has SPI and I2C outputs available, for this design the SPI is used to allow use of the highest sample rates available. The range is register selectable, with the widest range (±64g) expected to be used in this application. The mechanical bandwidth is about 8 kHz for the axes in the plane of the PCB, and 5 kHz for the axis perpendicular to the PCB. UTCRS accelerometers are typically mounted such that the axis of interest (radial with respect to the axle) is in the plane of the PCB.

The sampling is timed internally, with the rate register selectable up to 25600Hz. The device has 16-bit resolution, equivalent to 1.95mg. The noise level specification is 1.6mg for 50 Hz data rate,

which is expected to scale to about 36mg when using the maximum available sample rate of 25600 Hz.

The internal clock does not have timing accuracy called out in the published specification; however, our application requires highly accurate sampling time for synchronization with other sensors. Ideally the synchronization would be to better than 50us, and it is expected that the difference between clocks on two different devices will result in a drift far in excess of 50 us over the period of a burst, which may last up to 4 seconds.

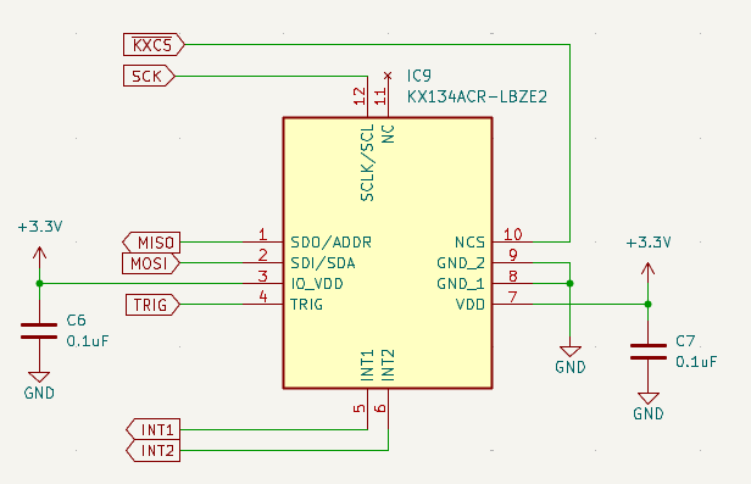

Figure 8: Main sensor board detail: Accelerometer and filter

(Version 3)

This timing drift will be accounted for using the INT1/INT2 pins on the KX134ACR-LBZE2, which can be configured to output a pulse every time data is ready. In addition triggering an SPI read of the KX134ACR data by the MCU, the number of interrupts are counted. The start and end times of the burst are set by the MCU and are accurate to ~10ppm, and the number of interrupts that occur during the burst can be used to calculate an accurate sample rate.

Thus to directly compare waveforms from two different sensors, the data will need to resampled (interpolated) to provide samples at precisely matched times. This adds a significant additional computation step, and is one major disadvantage of using a self-timed digital output accelerometer. The other disadvantage is inability to customize increase filtering to address aliasing. There is filtering included on chip and the accelerometer element has a rolloff at 8 kHz; however, if there are vibration frequency components above the sample rate that are strong enough to overcome

these there is no way to address them. In previous research UTCRS has found that strong signals above the range of interest for bearing defect detection were sometimes present and could alias into the desired range unless a high order filter was used. We intend to partially address this by sampling at the highest available rate (25600 Hz) and employing digital filtering in the data processing.

The disadvantages of the digital accelerometer should be considered in relation to its significant advantages. The digital accelerometer used here has an order of magnitude lower cost than the analog device plus filter used in the other versions, a much lower parts count, and the option to greatly reduce power consumption by lowering the data rate if spectral analysis is not needed.

4.5 Analog-to-Digital Conversion

The ADC portion of the main sensor board is shown in Figure 9. IC4 is an ADS8334E by Texas Instruments. It is a single 16-bit successive approximation register (SAR) with an 8-channel analog multiplexer. Thus, it can only read one of its eight input channels at any given sample. It uses the same clock signal (IC4 pin 19) for the SPI and to clock the SAR. When the chip is selected by bringing (IC4 pin 18) low, the first eight clock cycles are used for a start bit, a 3-bit channel selection. After that, 16 clock cycles are used to simultaneously clock the SAR and stream out the result bits as they are determined. It requires at least 24 clock cycles per conversion, and the maximum sample rate is 100 ksps (kilosamples per second), which would require the MCU to produce a >2.4MHz SPI clock. However, it is not anticipated that the ADC will be run at a sample rate of more than 25 ksps. When using an analog accelerometer, the sample rate is typically set at 2.5 times the accelerometer filter cutoff to barely clear the Nyquist frequency. This is because, for a given feasible number of samples per shot, and with adequate anti-aliasing filters, the benefits of spreading the shot over a longer time outweigh any benefits of oversampling. The longer shot time gives better frequency resolution and captures a larger number of wheel impacts. The maximum number of feasible samples per shot may be limited by available memory, or if the data is to be uploaded, by the amount of energy consumed by the upload.

In Version 3, using the digital accelerometer, the ADC is used only for temperate and load. These do not require high sample rates (at most 100 Hz); however, the same ADC is used in case external devices are attached requiring higher rates. External devices can be connected via J5.

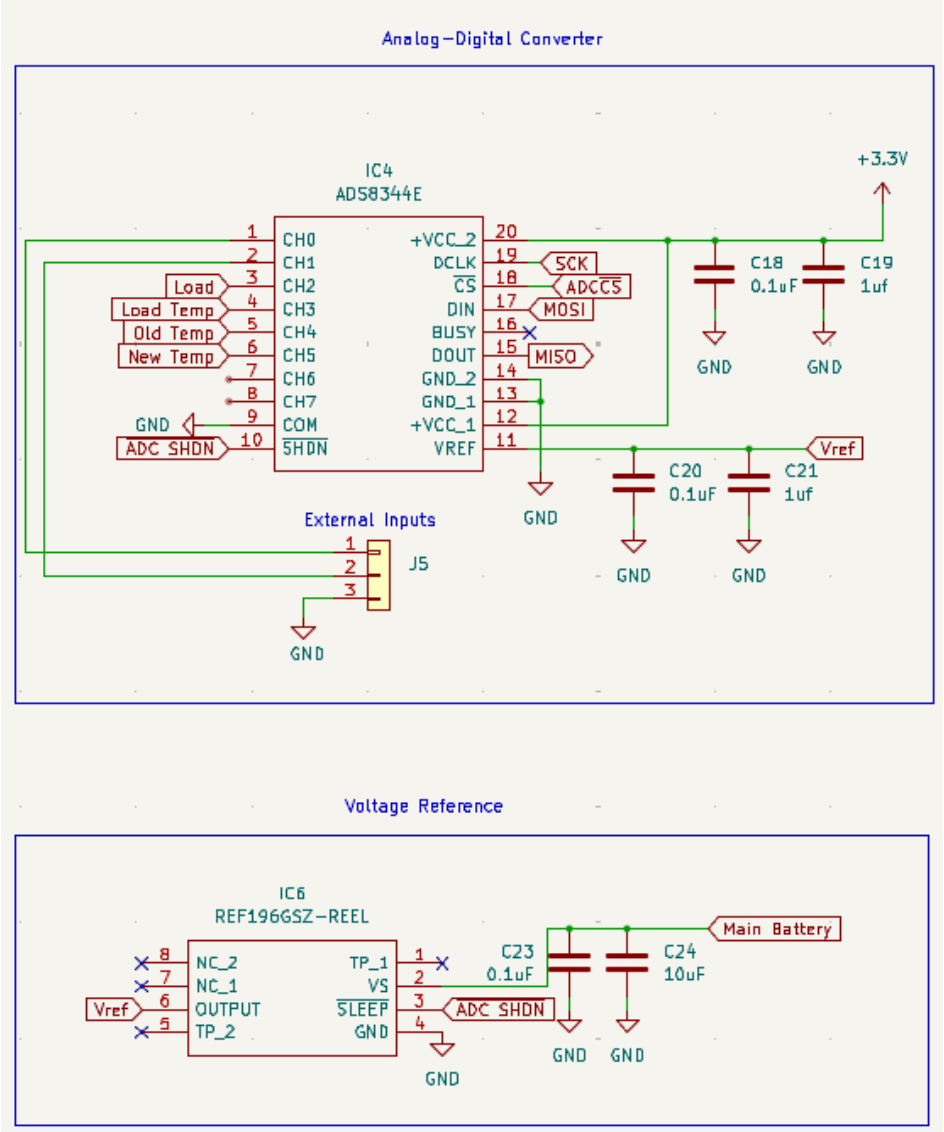

Figure 9: Main sensor board detail: Analog-to-digital conversion

(Version 3 shown. Versions 1 and 2 have CHO and CH1 connected to the raw and filtered analog accelerometer outputs, which are not applicable in this version.)

4.6 Load Sensor Signal Conditioning

The load cell amplifier is shown in the top half of Figure 10. As stated above, the load cell is not directly required for bearing health monitoring and may or may not be used depending on application. The load cell itself is located off-board, and in the current configurations used by UTCRS consists of a standard bridge-type strain gauge (350Ω) with an analog bandgap-type semiconductor temperature sensor (10mV/ºC) mounted in the same fixture. The separate load cell

temperature measurement is needed to compensate for changes in the calibration factor relating load to strain. The load cell assembly, if used, connects to the main board through connector J1 and provides a differential signal that is typically less than 10mV riding on a common mode offset of $V_{DD}/2$. A precision instrumentation amp, IC7 in the schematic, has high CMRR (100dB for the INA333 amplifier used) amplifies only the difference, and then places the zero-reference position back at one half of the supply voltage, so that at zero load it will be a midscale on the analog-to-digital converter. The voltage divider R4/R5 followed by voltage follower IC9 provides $V_{DD}/2$ to the reference pin at low impedance; failure to use a low impedance reference would degrade the common mode rejection.

4.7 Temperature Measurement

The board has two options for temperature measurement. U3, shown in the middle section of Figure 10, is an LM84 type semiconductor bandgap sensor with a useful range of -50 to 150ºC. The output scaling is -5.5mV/ºC with 1.034V offset at 0ºC. In previous generation wireless sensor designs, a sensor of this type was mounted on the backside of the PCB to obtain a direct contact between the sensor package and the bearing adapter surface when the PCB was mounted. However, it was found that this arrangement created a bending stress on the PCB when clamped, and due to the plastic case on the LM84, the thermal resistance was still relatively high. If not used, this device can be left unpopulated.

The second option is a resistance temperature detector (RTD), shown in the bottom section of Figure 10. The RTD to be used is a platinum thin film device, NB-PTCO-050, with a nominal resistance at 25ºC of 1000Ω. It is a two terminal leaded device with a small (1.2mm×4.0mm) ceramic substrate. The solder pads for the RTD leads are located at the edge of the PCB, with the RTD substrate off the edge of the board and in direct contact with the adapter surface. The substrate has a tab extension that can be clamped under the head of a mounting screw. It is read using a simple voltage divider connected to one channel of the main board's analog-to-digital converter. The resistance-versus-temperature curve is non-linear and will need to be programmed in firmware.

Both sensors are powered by a dedicated voltage regulator (see Section 4.3) that is disabled when the sensors are not in active use.

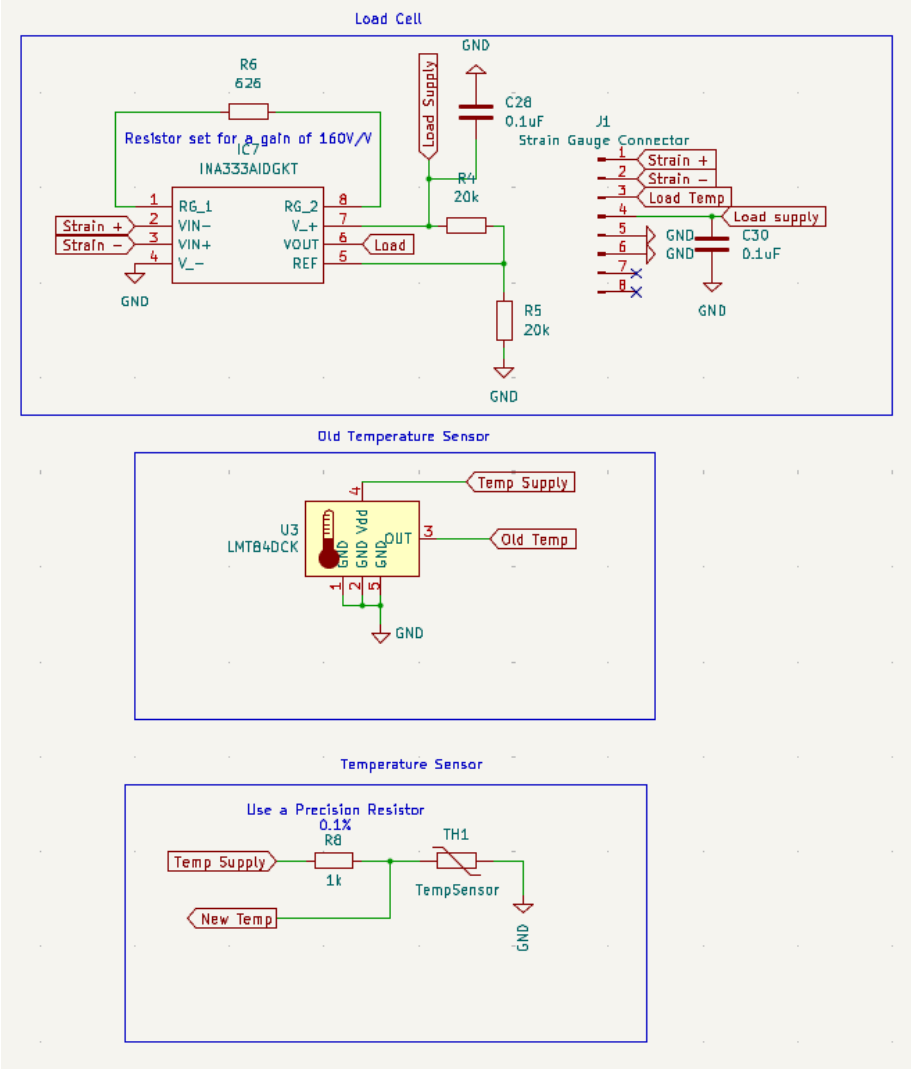

Figure 10: Main sensor board detail: Temperature and off-board load cell (Version 3)

4.8 Interface to Daughterboards

The interfaces to the two daughterboards are shown in Figure 11. J3 is the connector to the battery management board, with pins 10 and 1 providing the main power and ground connections, respectively. While pin 10 is labeled “Main Battery”, in actual use it is attached to the main energy storage device, which could be a battery, supercapacitor, or hybrid. A voltage divider allows the MCU to monitor state of charge. Pins 2 and 4 can be used to monitor various aspects of the energy harvesting system. There are two separate signals to allow separate monitoring in cases where there are two harvesting devices (e.g. two thermoelectric generators (TEGs) or two solar cells).

J4 is the connector to the communications daughterboard. Pins 3, 5, 7, and 9 are labeled for SPI communications, but could be reconfigured in MCU firmware for UART or I^2C format. Pins 2,4,6,8 are also firmware configurable. The current intent is to use Pin 2 for resets to the communications board, while Pins 4, 6, and 8 would normally be configured to receive hardware interrupts and/or status pin signals from the communications board. As mentioned earlier, hardware interrupts may be used to precision trigger the start of vibration measurement sequence by the MCU.

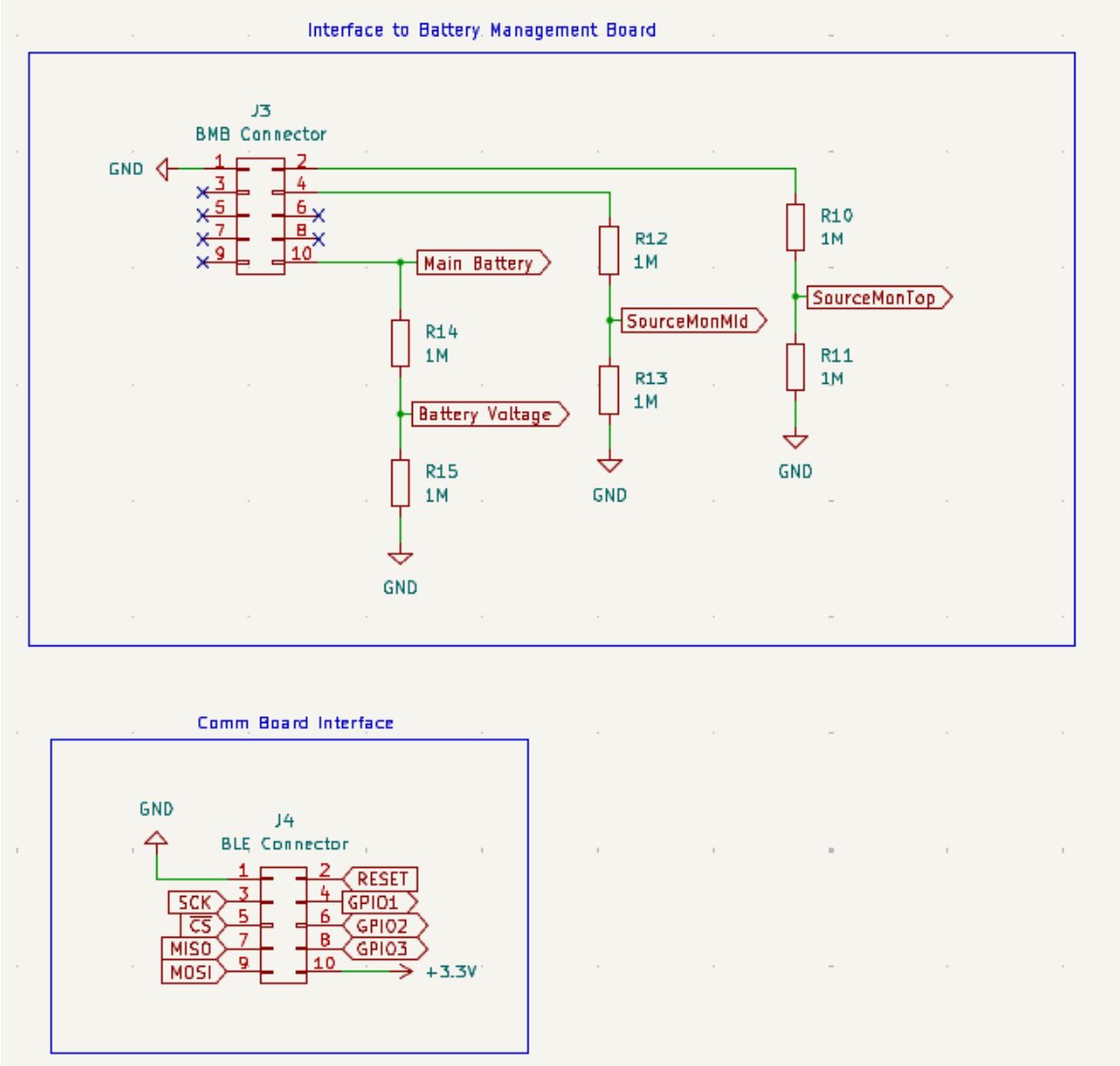

Figure 11: Main sensor board detail: Interface to daughterboards (Version 3)

4.9 Main Board PCB Layout and Fabrication.

The layout for the current main board is shown in Figure 12, and an earlier version of the fabricated board with annotations is shown in Figure 13. The board parameters are 63.5mm×31.8mm, four layers, FR-4 TG150 substrate, 1 ounce copper, 1.6mm total thickness. No traces or clearances of less than 0.006 inches (0.15mm) are used, making the board suitable for low-cost production.

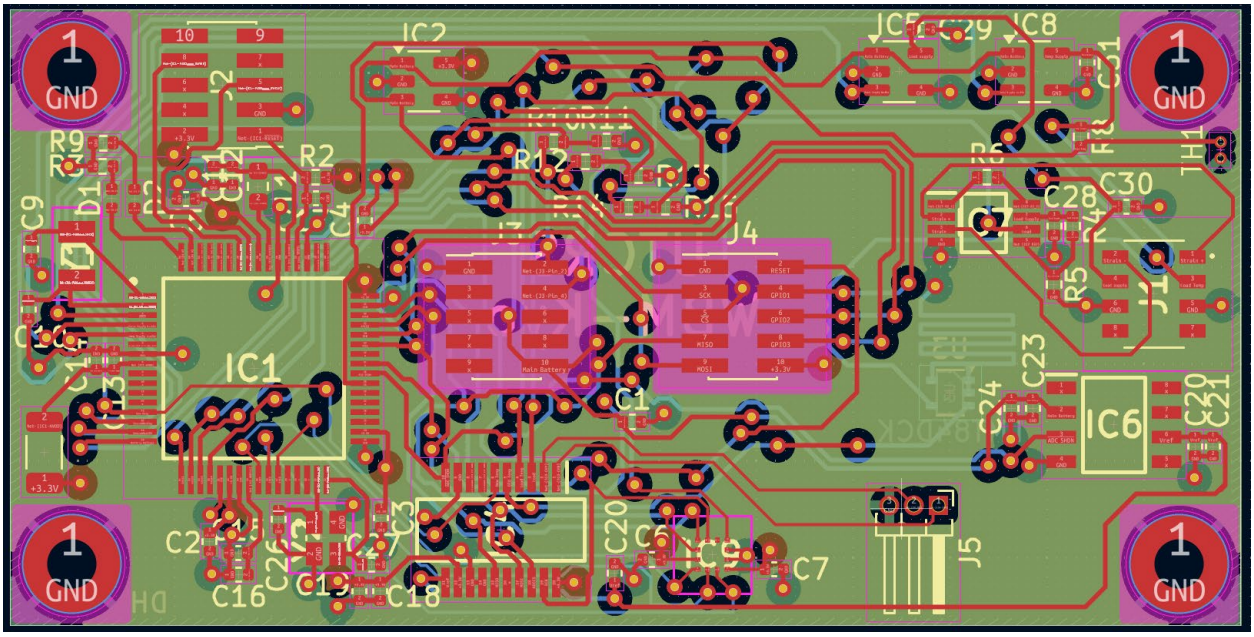

Figure 12: Main sensor board PCB layout (Version 3 shown)

4.10 Main Board Status

Version 1 has been assembled and tested. Initial testing has been completed verifying ability to flash the MCU and run test firmware communicating with peripherals. During the testing, issues needing correction were identified; in particular, an improved drive circuit for the reference pin of the instrumentation amplifier in the load sensor conditioning. Despite these issues, the board is suitable for continued use while the second revision is under fabrication, and firmware is currently under development.

Version 2: A second revision, incorporating the hardware changes mentioned above, has completed blank PCB fabrication and is awaiting final assembly.

Version 3: The third version has been sent for PCB fabrication.

A bill of materials and links to obtain CAD files are given in the Appendix.

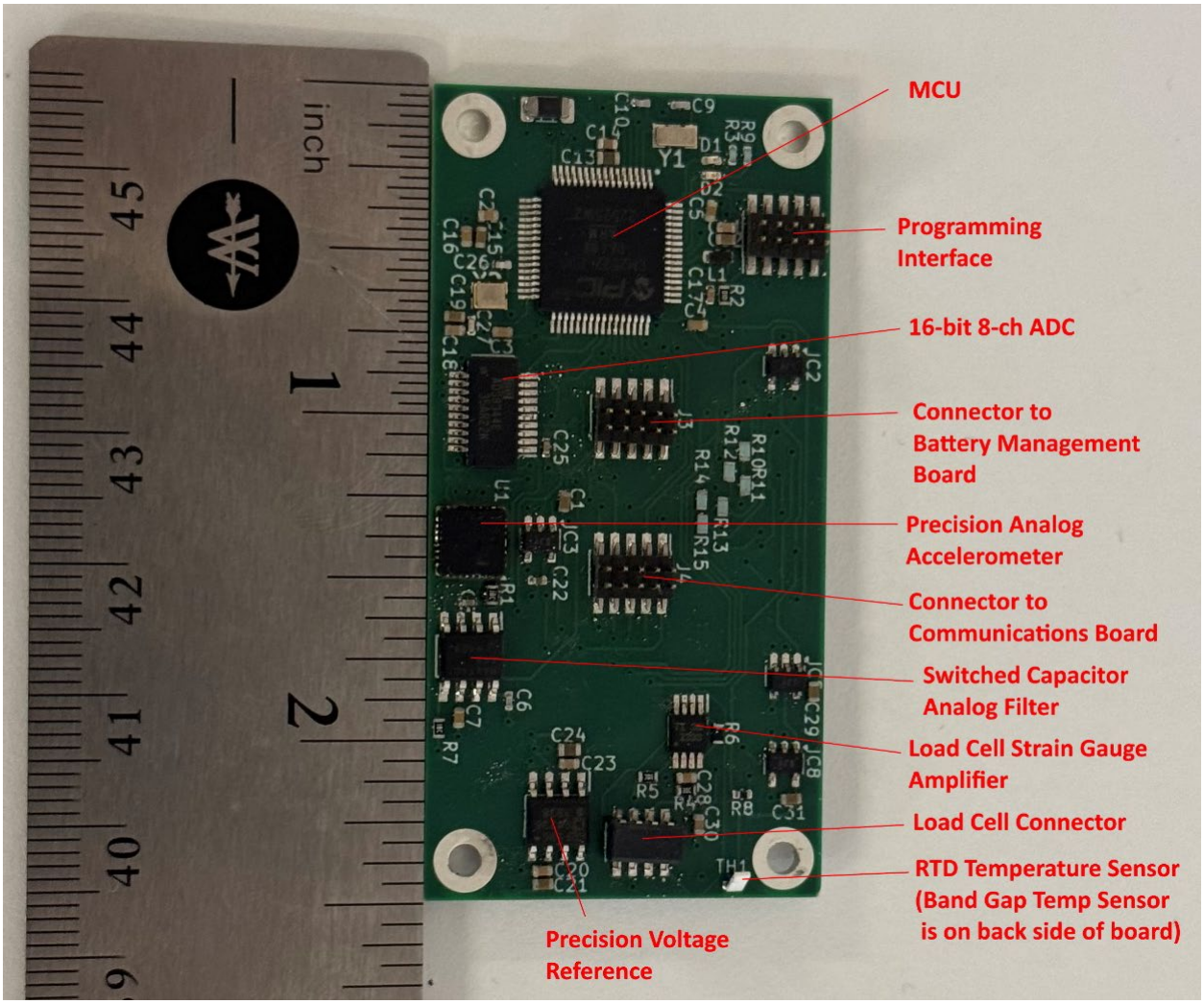

Figure 13: Fabricated main sensor board (Version 1 shown)

5 Communication Boards

5.1 Overview

Two versions of the communication board have been designed and fabricated. One version targets the 902-928 MHz band using LoRa communication protocols; the other targets the 2.4-2.48 GHz band using BLE or mist™ communication protocols. However, both have some flexibility to modify frequency bands, modulation, and packet structure.

Each board is based on an RF-enabled general-purpose microcontroller rather than a dedicated transceiver integrated circuit. This gives each board the ability to run firmware independent of the main board, as well as access to basic peripherals such as hardware timers. While this increases parts count and hardware complexity, it simplifies independent firmware development for each module and greatly increases flexibility to "swap out" new communications hardware. This approach has relatively little impact on power consumption, since the total current draw of an RF-enabled microcontroller is strongly dominated by the transceiver and transmitter when communications are active. The addition of a general-purpose core adds only a small percentage to the daughterboard power.

5.2 Communication Board - LoRa Version Circuit

The schematic of the LoRa version of the communication board is shown in Figure 14. It is based on an STM32WL55C processor that includes both an Arm Cortex M4 core and an on-chip RF transceiver capable of 150-960 MHz operation using LoRa, FSK, MSK, or BPSK modulation. In a simpler system, the Arm Cortex M4 could have sufficient computational and I/O resources to implement an entire single-MCU wireless sensor, and this solution could be more cost effective in commercial applications. However, as discussed in Section 3, a decision was made to use a separate mainboard MCU for collecting and processing data from the analog sensors. In a research platform, this will facilitate parallel research and development efforts in data collection, signal processing, and communication protocols. It is anticipated that when demonstrating a long-battery life system, the STM32WL55C will be shut down except for scheduled communications windows with a duty cycle of less than 1%, while the low power PIC32CM3532 on the mainboard will have a higher duty cycle to poll sensors.

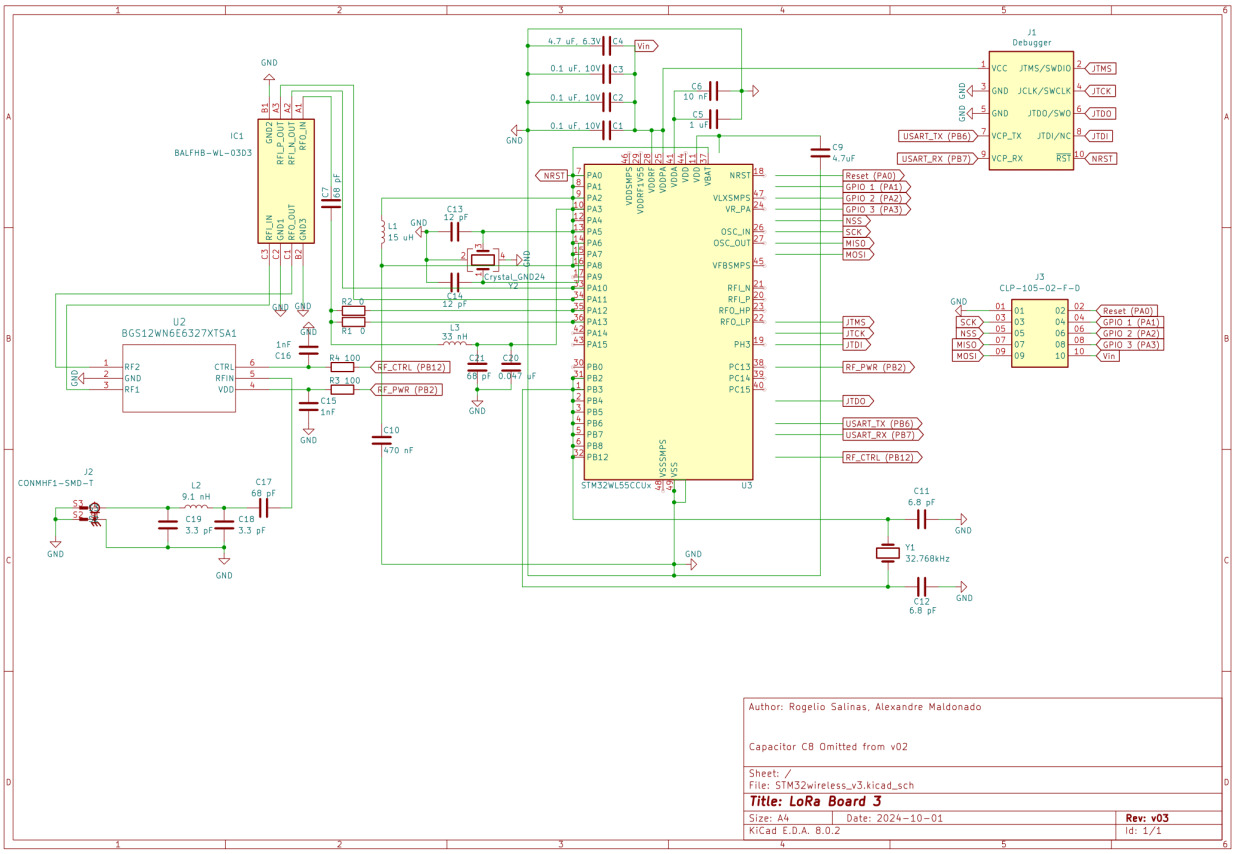

Figure 14: Schematic of Communications Board (LoRa Version)

(Note: This high-resolution image can be zoomed for enhanced detail)

An enlarged view of the RF section of the LoRa version is shown in Figure 15. Significant off-chip matching, balun, and switching circuitry is required, and needs to be optimized for a particular frequency band, in this case 902-928 MHz. As noted above, the STM32 transceiver is capable of 150-960 MHz but use of other bands within its range would require redesign of the external circuitry. The antenna (connector J2) is fed through a lowpass filter formed by C18, C19, and L2. U2 is an RF transmit-receive switch under the control of the STM32. IC1 is a specialized matching and balun network supplied by STM Microelectronics specifically for use with STM32W55C MCUs. It has separate receive and transmit paths. The antenna side of both paths is unbalanced, while on the MCU side, the receive path is balanced and the transmit path is unbalanced. The STM32 has two different RF output stages, one high power and one low power. In fabrication only, one is selected by populating either R1 or R2, but not both.

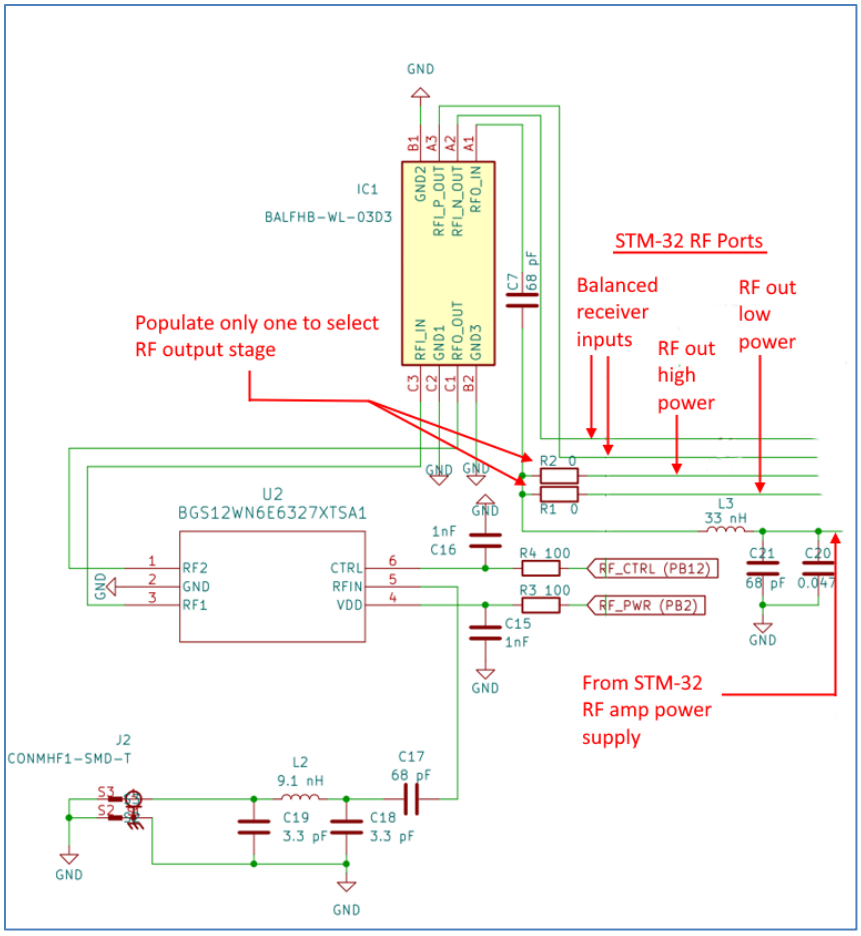

Figure 15: Communications board detail: LoRa version RF section, Revision 3

The interface to the mainboard is through connector J3 in Figure 16. Pins 3, 5, 7, and 9 are an SPI interface. Pin 10 is 3.3V supplied from the main board. Pins 4, 6, and 8, designated as GPIO pins, can be used for unspecified functions. One intended use is to allow immediate hardware interrupts from the communications board STM32 to the main board PIC32 when reception of a broadcasted timing synchronization packet has been completed. This should facilitate precision synchronization of sample times across multiple wireless sensor units. Other potential uses are PIC32 to STM32 interrupts for more precise control of transmit packet start times, and rapid monitoring of the STM32 status by the PIC32 without the need for reading status registers over the SPI.

The other connector (J1) in Figure 16 is the SWD programming interface for the STM32 MCU, as well as a UART interface for debugging purposes. It does not connect to the main board.

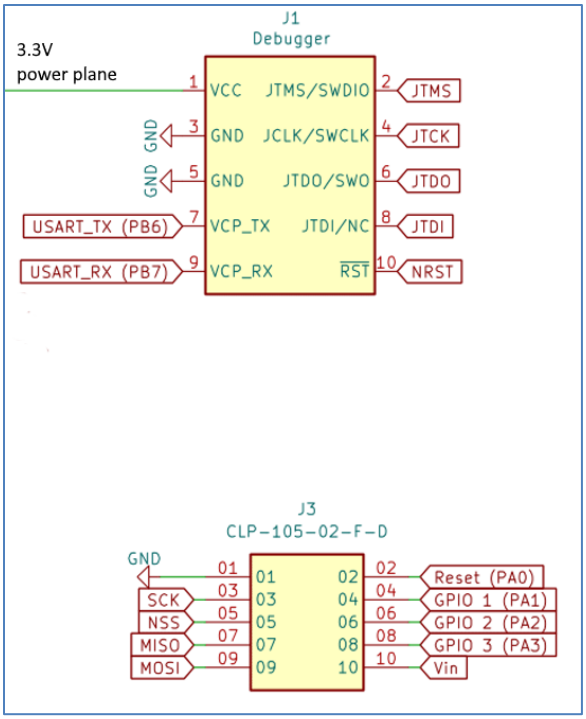

Figure 16: Communications board detail: LoRa version main board interface, Revision 3

5.3 Communication Board – LoRa version PCB, Fabrication, and Status

The printed circuit layout for the latest revision of the LoRa communication board is shown in Figure 17. The board measures 31.8×30.7mm, has four copper layers, and is on FR-4 substrate with a total thickness of 1.6 mm. The third revised version is shown in the figure. A fabricated example of the second revision (the latest one completed at the time of the report) is shown in Figure 18, with important components identified. The MCU portions have been successfully tested for basic functionality and ability to run test firmware. An issue with RF power amplifier bias circuitry was identified and the corrected design, Revision 3, is in PCB fabrication. Firmware for the sensor application is under development.

A bill of materials and links to obtain CAD files are given in the Appendix.

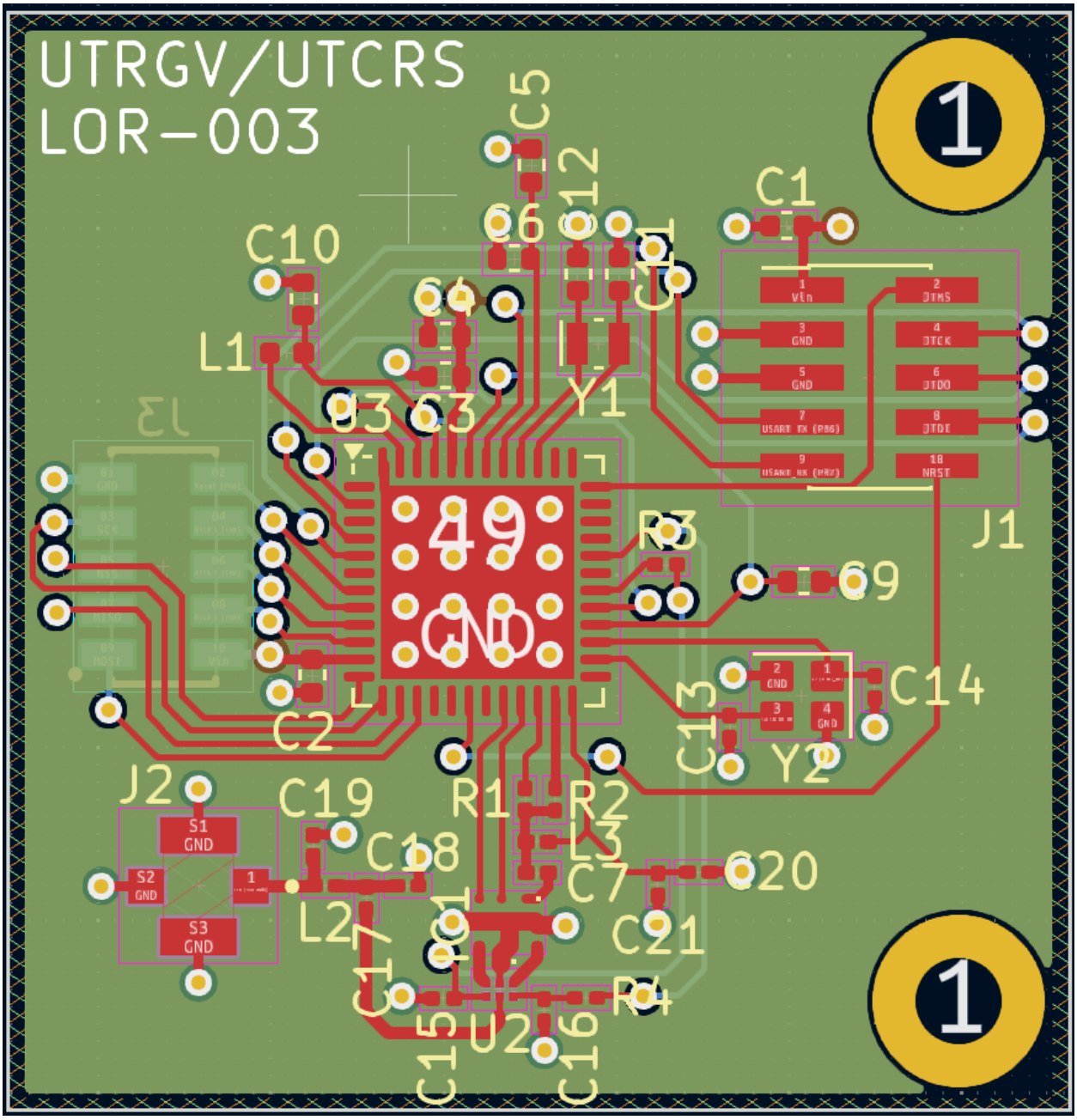

Figure 17: Communications board PCB layout (LoRa version, Revision 3)

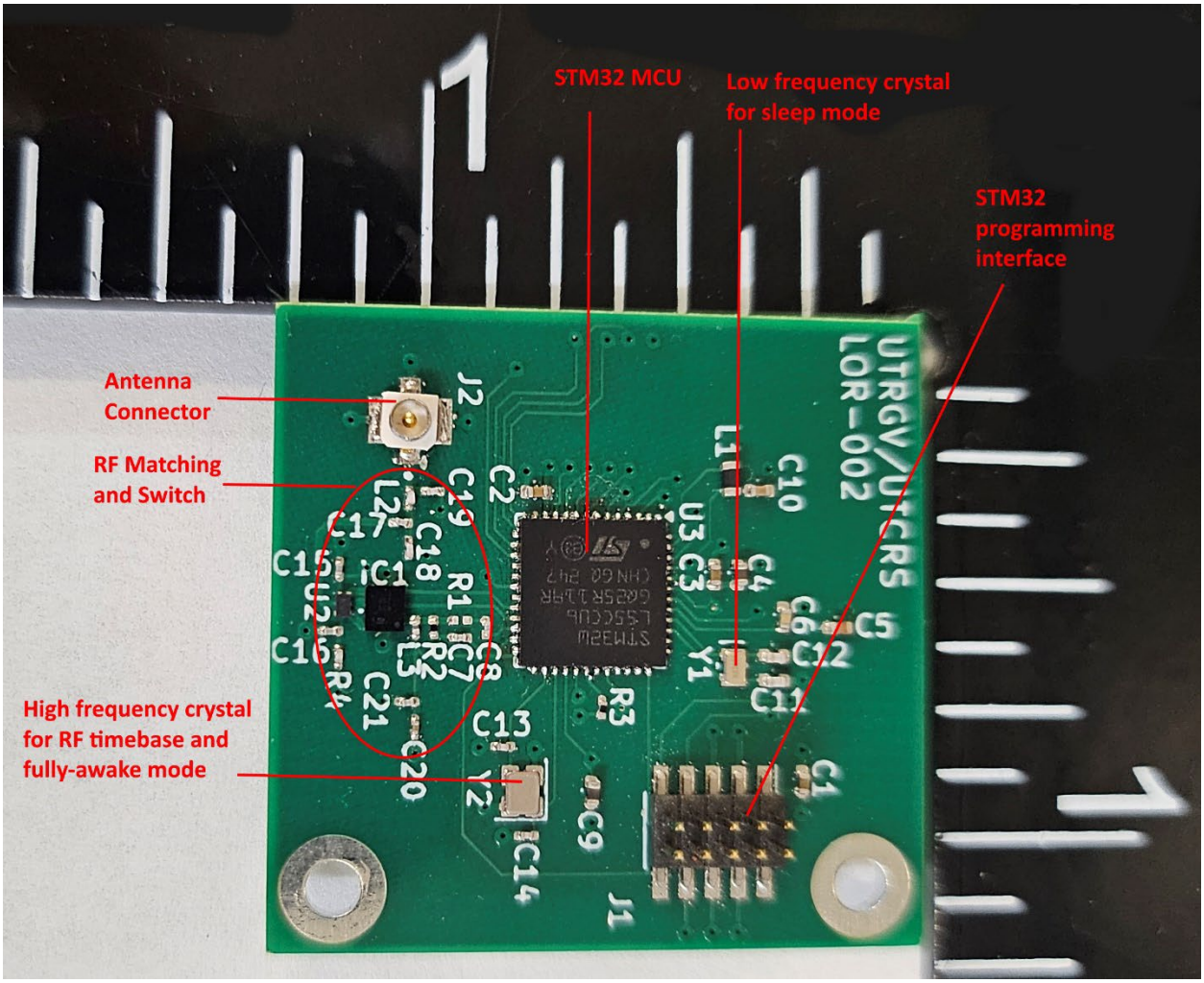

Figure 18: Fabricated communications board (LoRa version, Revision 2, annotated)

(The connector to the main board is on the bottom side of PCB)

5.4 Communications board (2.4 GHz Version)

The schematic diagram for the 2.4 GHz version is shown in Figure 19. It is based on the Nordic nRF52840, an MCU with an ARM Cortex M4 and on-chip RF module intended to operate in the 2.4-2.48 GHz ISM band using Bluetooth Low Energy (BLE) and IEEE 802.15.4 specifications. One intention of this project is to evaluate BLE and mist^{TM} protocols, which have firmware stacks available. These stacks handle pairing with other devices and forming ad-hoc networks. While this capability makes initial development easier, it also results in reduced end-user control of exactly when packets are sent and received. This may not be suitable for some of the data collection

methods that were described in Section 2. The nRF52840 also has capability for user-defined protocols that may give greater control at the cost of increased firmware development.

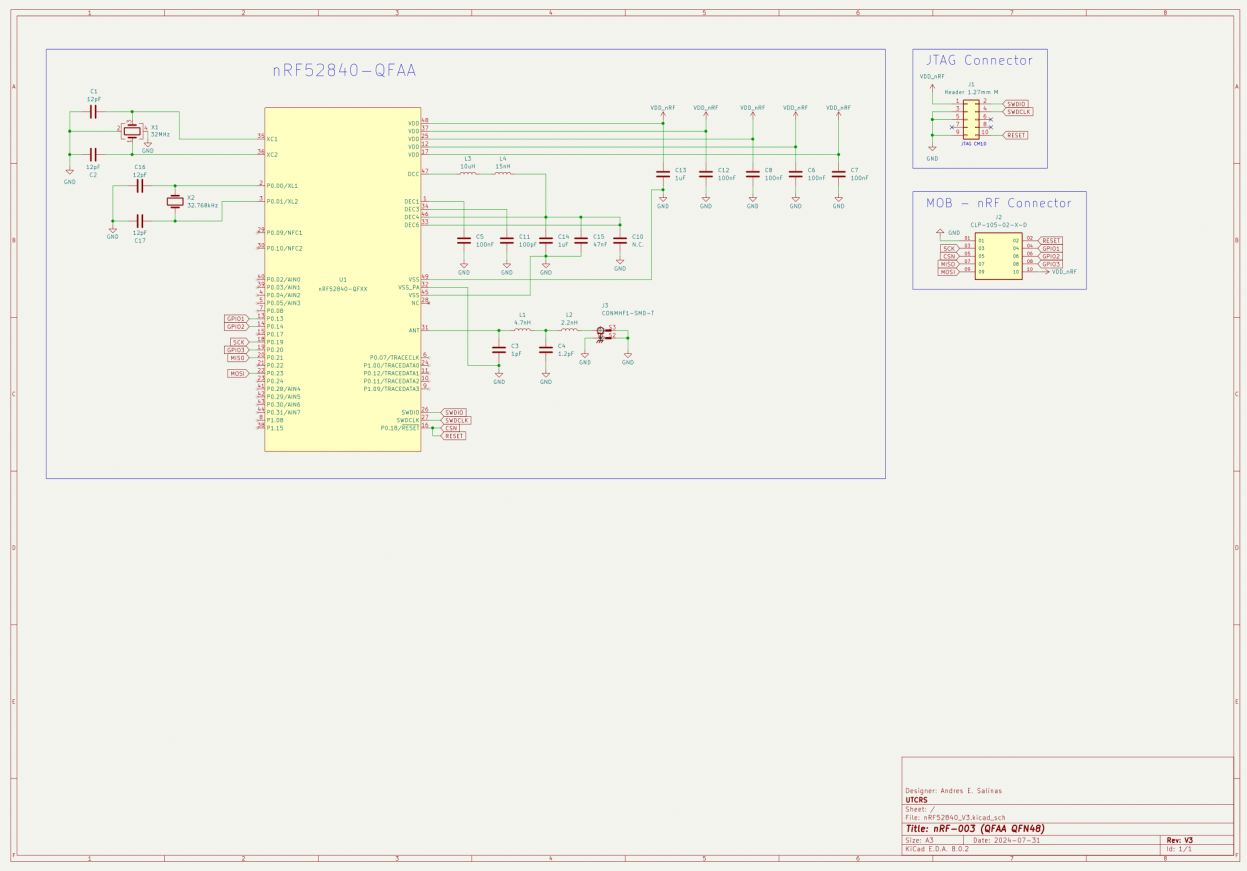

Figure 19: Schematic of Communications Board (2.4 GHz Version)

(Note: This high-resolution image can be zoomed for enhanced detail)

5.5 Communication board – 2.4 GHz circuit

Clock and I/O pin connections for the MCU are shown in Figure 20. There are two clock oscillators with external crystals, one HF clock at 32 MHz (crystal X1) and another LF clock at 32.768 kHz (crystal X2). The HF oscillator is the general system clock when the MCU is awake and running at full speed. It also provides an accurate timebase for PLL generation of the RF transmit and LO frequencies used for 2.4-2.48 GHz communications. The LF clock is used primarily to increment timers when the MCU is in timed sleep mode. In the current version of the circuit, a standard accuracy (20ppm) crystal is used which is sufficient for BLE applications. To use the mist™ protocol, which depends on precision windowing to reduce power consumption, crystal X2 would

need to be upgraded to a higher accuracy unit, and the loading capacitors C16 and C17 changed as appropriate for the new crystal.

As stated earlier, for BLE applications, we plan to use the SPI interface (pins 18, 20, 22) to communicate with the main sensor board. However, for mist^{TM} modem applications, the MCU pins on both this board and the main sensor board can be reassigned to the internal UARTs on each MCU.

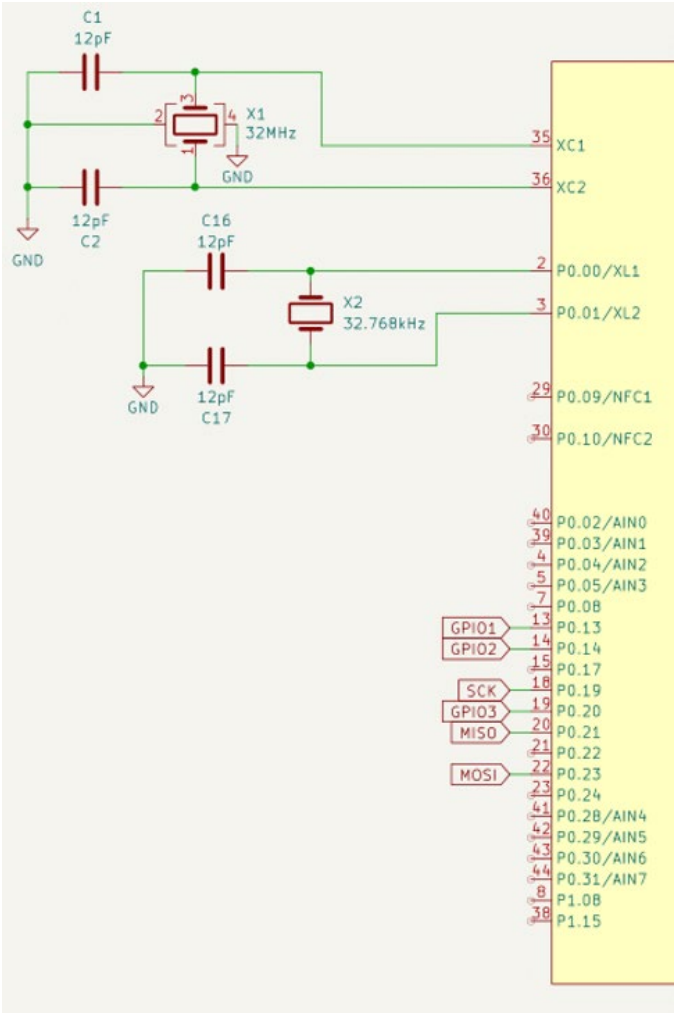

Figure 20: Communications board detail: 2.4 GHz version MCU

Most of the required circuitry for RF functionality is provided on-chip; the only external components needed are for a combined impedance matching and low pass filter circuit as shown in Figure 21. This circuit is taken directly from the Nordic semiconductor reference design; the only modifications are to the PCB layout.

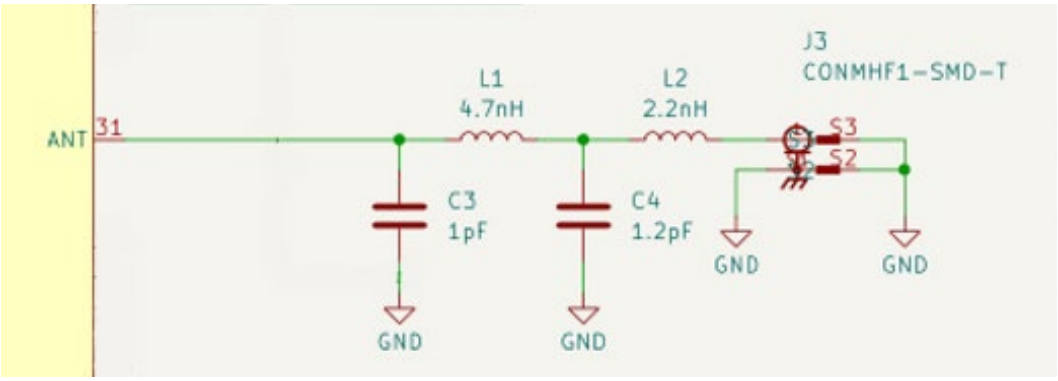

Figure 21: Communications board detail: 2.4 GHz version RF section

The connection to the mainboard is through connector J2 shown in Figure 22. The pinout is compatible with that for the LoRa communications board, with pins 3, 5, 7, and 9 used for an SPI interface. However, the corresponding pins on the nRF52840 and PIC32 on the mainboard can be reassigned in firmware as UART pins. This mapping can be used if the nRF52840 is configured as a mist™ modem using serial AT-style commands.

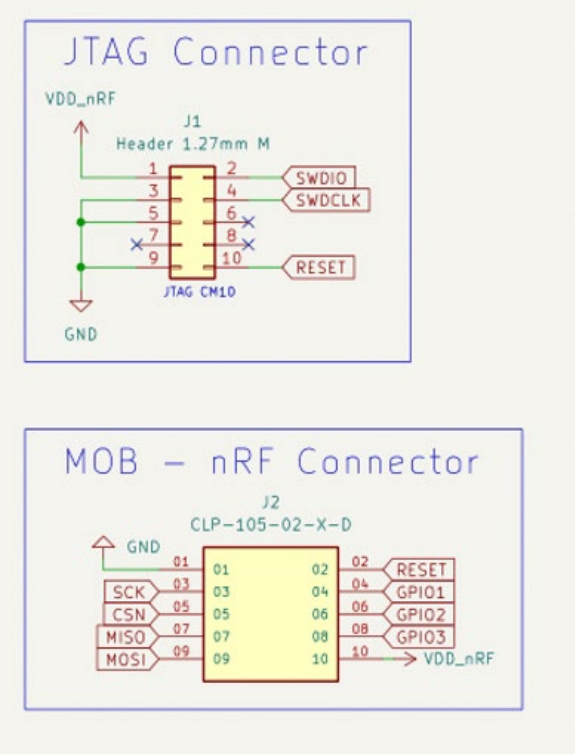

Figure 22: Communications board detail: 2.4 GHz version main board interface

The other connector (J1) in Figure 22 is for JTAG programming of the nRF52840. It does not connect to the mainboard.

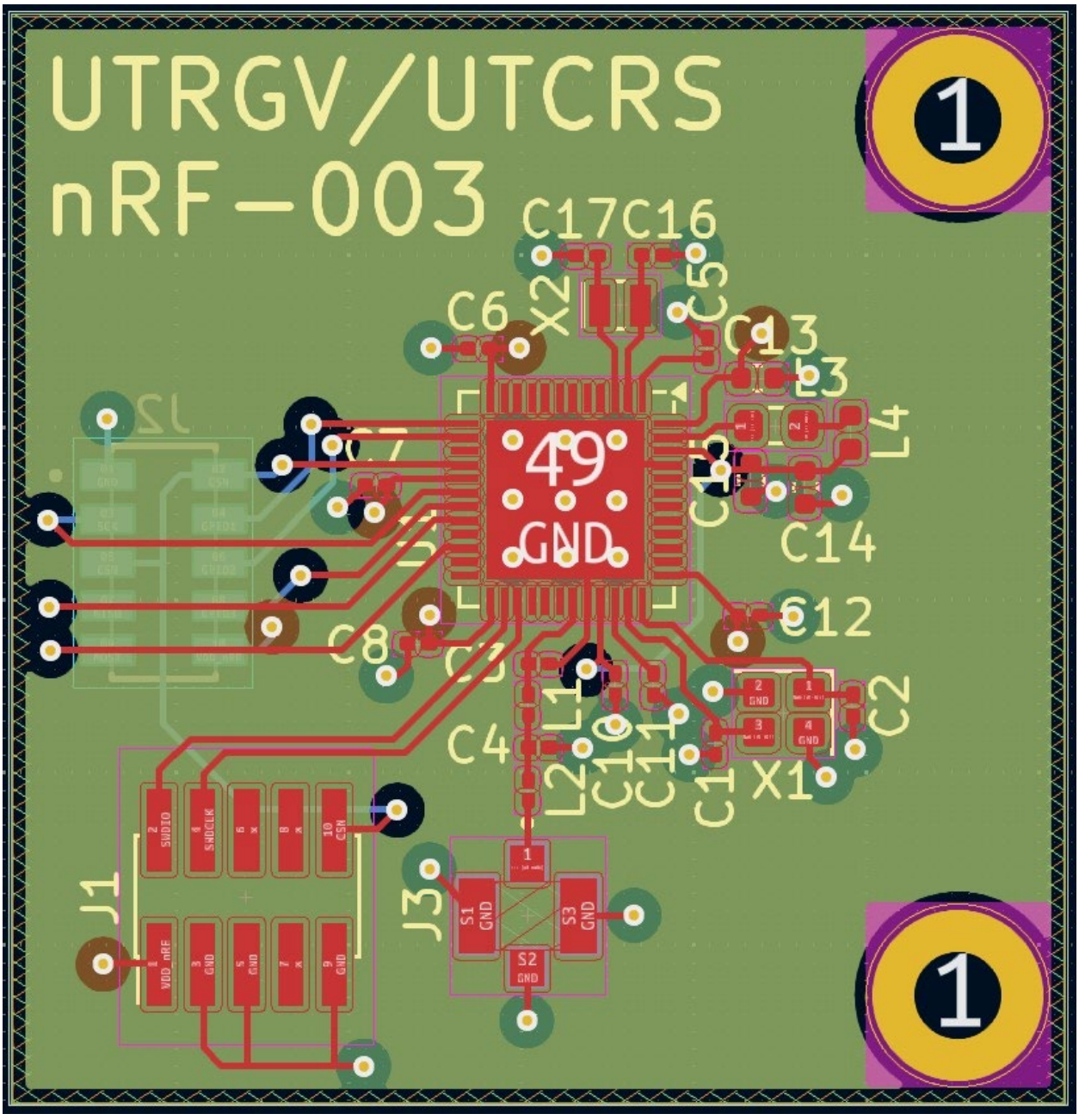

Figure 23: Communications board PCB layout (2.4 GHz version)

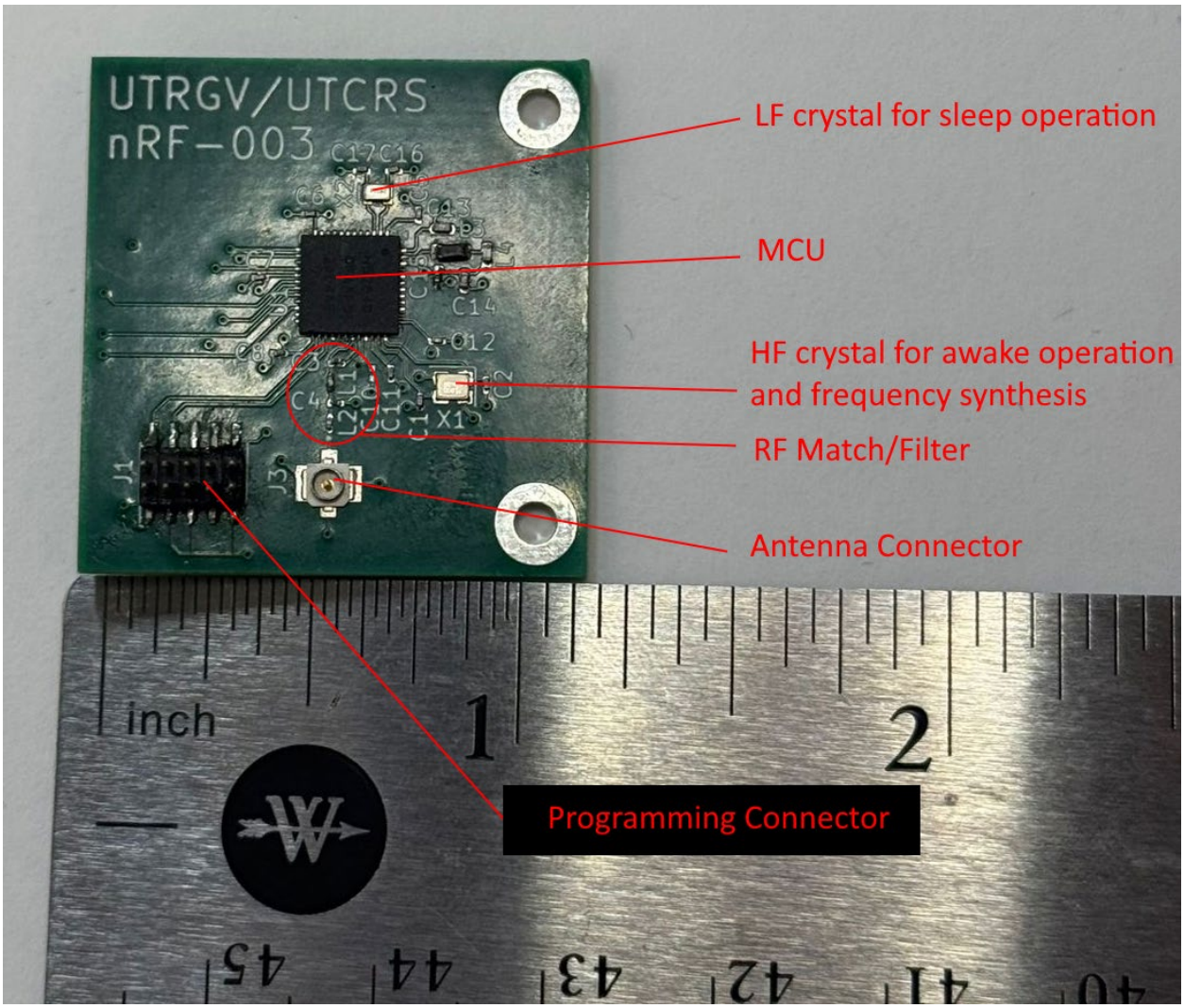

Figure 24: Fabricated communications board (2.4 GHz Version, annotated)

(Connector to main board is mounted on the backside of the PCB)

5.6 Communication Board – 2.4 GHz PCB, fabrication, and status

The printed circuit layout for the latest revision of the 2.4 GHz communication board is shown in Figure 23. The board measures 31.8×30.7mm, has four copper layers, and is on FR-4 substrate with a total thickness of 1.6 mm. A fabricated example is shown in Figure 24, with important components identified. The board has been successfully tested as a generic BLE beacon. Firmware for the sensor application is under development.

A bill of materials and links to obtain CAD files are given in the Appendix.

6 Battery Management Boards

The battery management board supports energy harvesting from a variety of sources, with the energy used to charge various storage devices including secondary batteries, supercapacitors, or hybrid battery/capacitor devices. It also allows low-dropout (LDO) switching to a primary battery as backup for the main storage device. The LDO regulators on the mainboard need at least 3.35 Volts from the battery management board for proper operation.

Two versions of the battery management board have been designed. One version is based on the E-Peas AEM20940, which has a cold-start voltage of about 380mV, a maximum input voltage of 3.5V. It is jumper and resistor programmable to operate in several different modes. The second version is based on the Matrix Mercury MCRY12-125Q42DIT, a lower cost device with superior input specifications (25mV cold start and 7V maximum input) but less flexibility in the operating mode and lower maximum charging rate.

The relative importance of a low cold-start voltage versus a high maximum charging rate depends strongly on the source being harvested and the charging strategy. Trickle charging from a weak source that is always available may need the ability to cold-start at low voltage levels; opportunistic charging from a strong source that is intermittently available requires a high maximum charge rate.

6.1 Battery Management Board – E-Peas version circuit

The schematic for the E-Peas version of the battery management board is shown in Figure 25. Most of the functionality is provided by a single integrated circuit U1, the AEM20940. As stated above, its cold-start voltage is a relatively high 380mV, while the device is damaged by inputs greater than 3V. It is capable of charging devices up to 4.2V, which is suitable for nominal 3.7V lithium cells. Depending on input and output conditions, it automatically switches between buck and boost modes. The configuration resistors (R1 through R6) can be selectively populated to control features such as maximum power point tracking (MPPT), maximum charge voltage, and charge balancing if two low voltage supercapacitors are used in series to obtain a higher voltage rating. The MPPT circuit can be programmed to operate at 50 or 55% of source open-circuit voltage, suitable for thermoelectric generators (TEGs), or 75% of source open-circuit voltage, suitable for solar cells. In cases of high available input power, the AEM20940 can charge at up to 80mA/550mW.

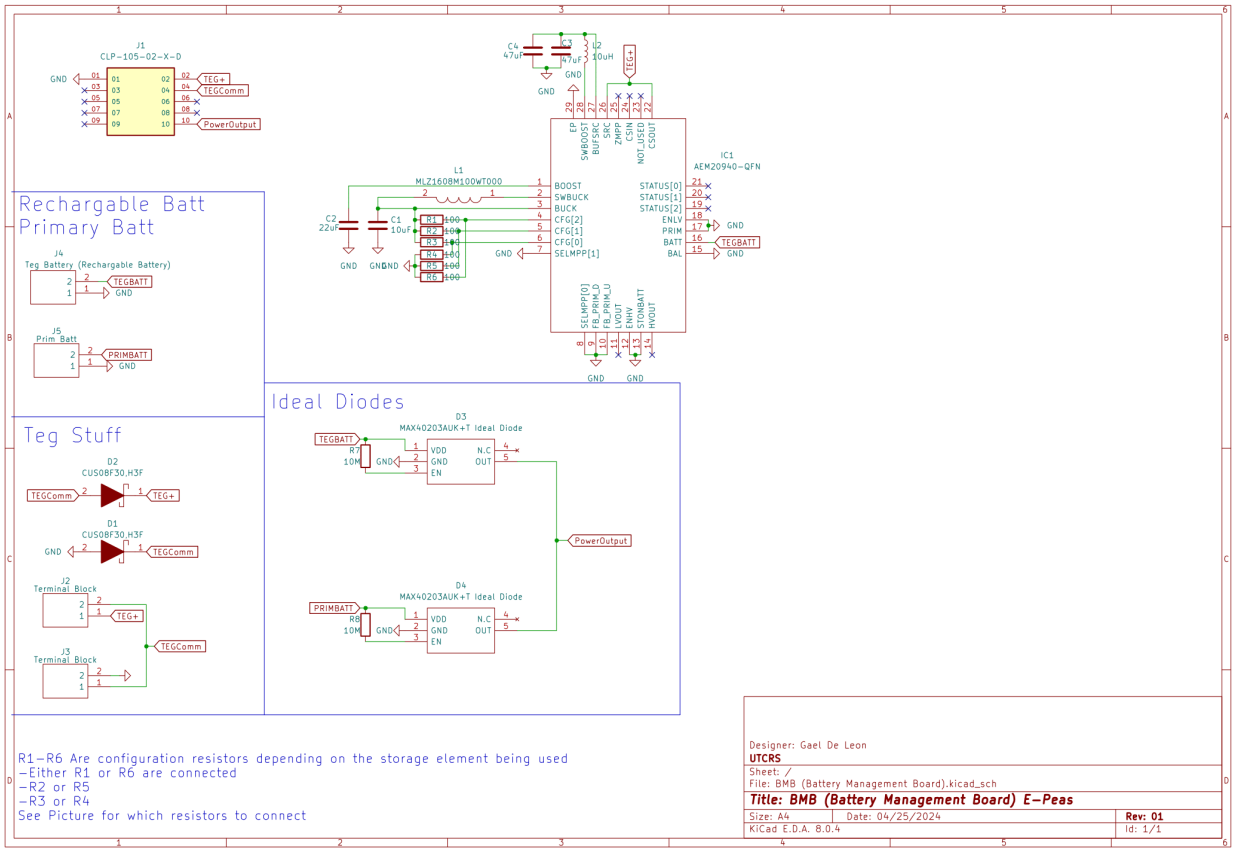

Figure 25: Schematic of battery management board (E-Peas version)

(Note: This high-resolution image can be zoomed for enhanced detail)

D3 and D4 are MOSFET based “superdiodes” which have a voltage drop in the 10’s of mV range and are used to switch to the primary battery when the storage battery or supercapacitor (net marked TEGBATT in the schematic) voltage falls below that of the primary. The box at the lower left is marked TEG but could be used for solar harvesting or the rectified output from an electromechanical harvester. The dual input connector and bypass diodes (D1 and D2, conventional Schottky diodes) are for use with two TEGs in series to overcome the cold-start limit at low temperature differences. The diodes are used to partially mitigate situations in which one TEG operating in generation (Seebeck) mode wastes energy in the series resistance of a weaker TEG, or even drives the other TEG in energy pump (Peltier) mode. This can occur if the two TEGs are operating at substantially different temperature differentials [10].

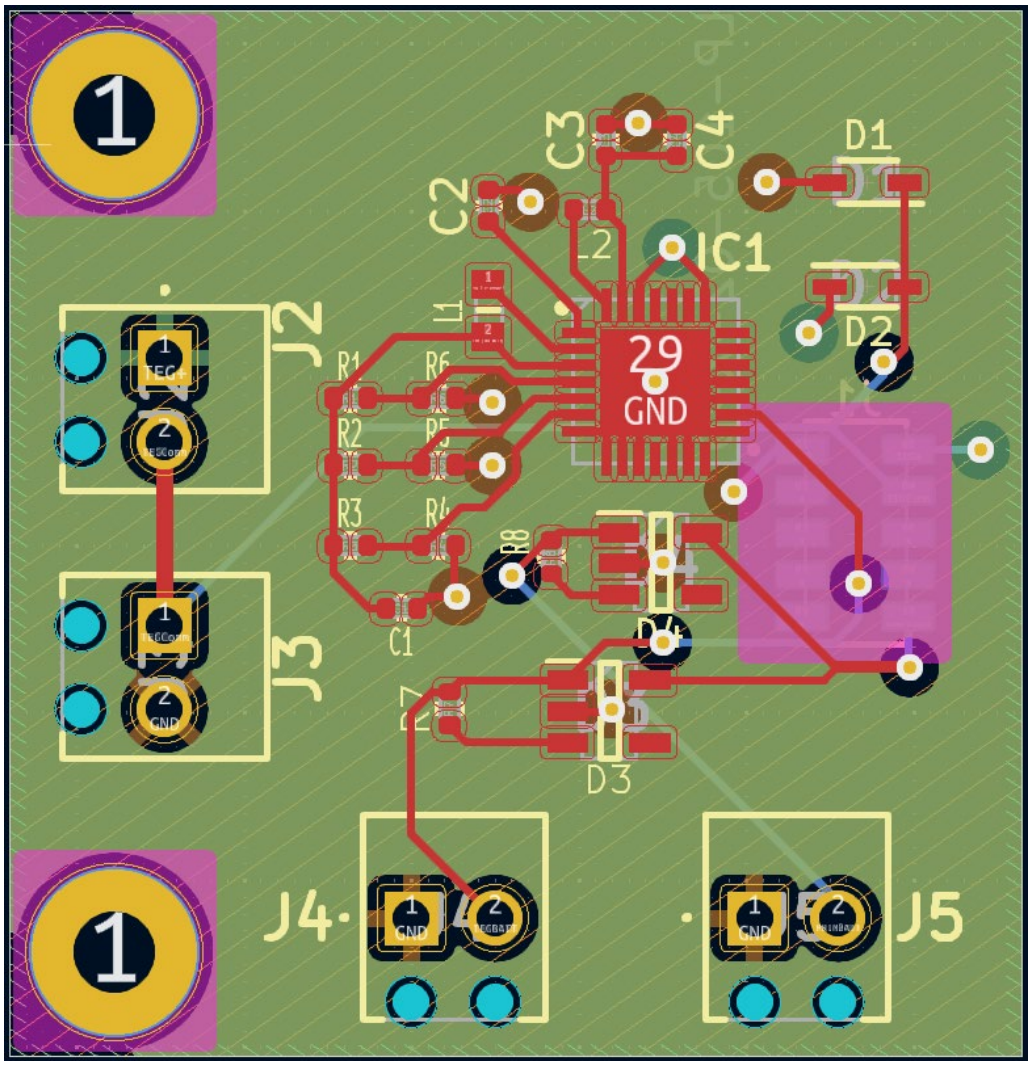

Figure 26: Battery management board PCB Layout (E-Peas version)

The connectors are as follows:

J1 – Connection to mainboard. Pins 1 (GND) and 10 (Power Output) are the power to the main board, drawn either from the storage device or the backup primary battery. When operating properly (i.e., either the primary or secondary battery has sufficient charge), the board should output between 3.35V and 4.2V. The lower limit is set by the dropout voltage for the regulators on the mainboard, while the upper limit is set by the maximum safe voltage for a single cell lithium-ion battery. The other connected pins (2 and 4) can be used to directly monitor the energy harvesting sources.

J2 and J3 – Connections for two TEGs operated in series. In cases where there is a single source, for example, a single TEG or a solar cell, it should be connected with the negative terminal to Pin 2 on J3 and the positive terminal to Pin 1 on J2, with the other pins left unconnected.

J4 and J5 – Connections for the storage device (TEGBATT) and primary battery, respectively.

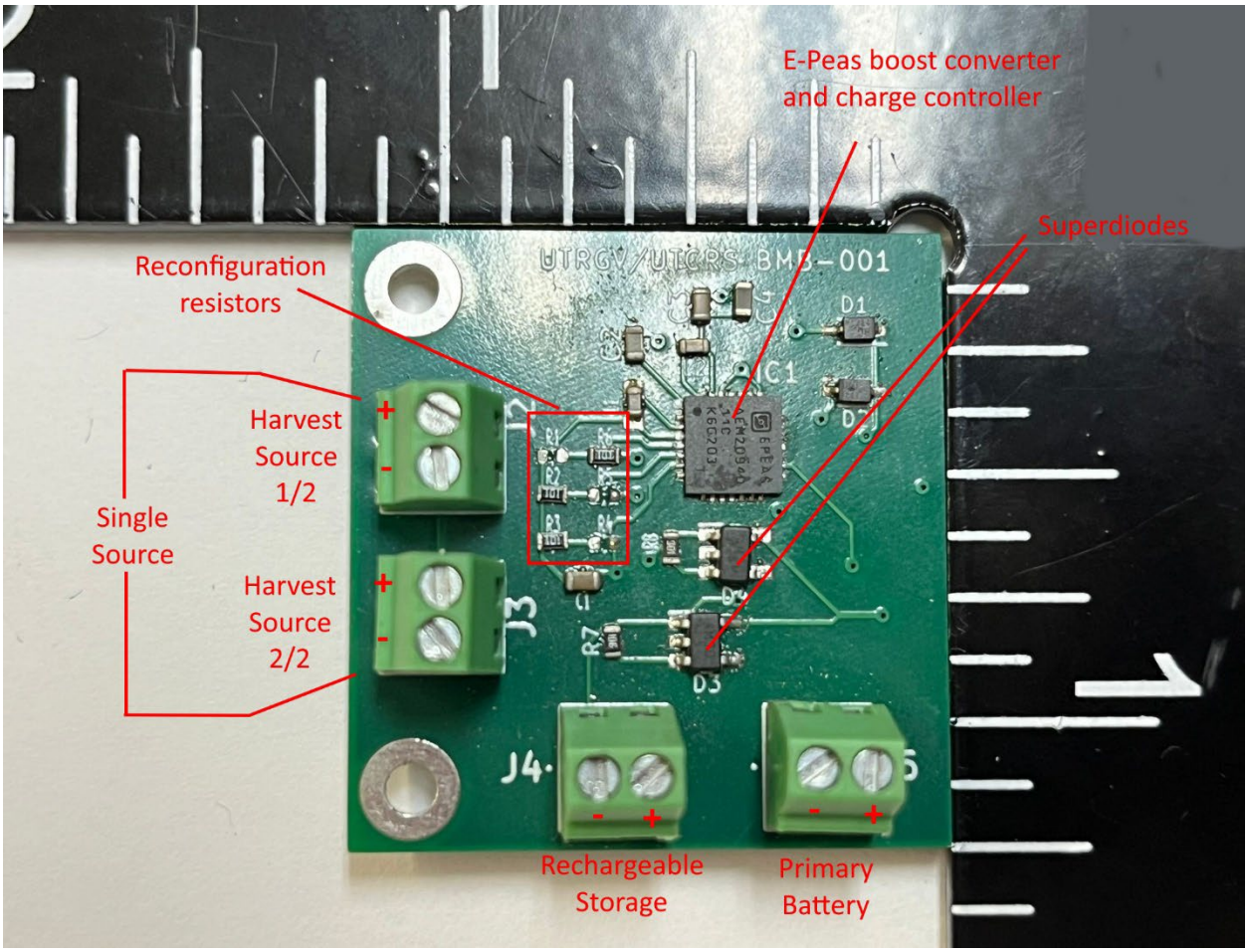

Figure 27: Fabricated battery management board (E-Peas version)

6.2 Battery management board – E-Peas version PCB, fabrication, and status

The printed circuit board layout for the E-Peas version of the battery management board is shown in Figure 26. The board measures 31.8×30.7mm, has four copper layers, and is on FR-4 substrate with a total thickness of 1.6 mm. A fabricated example is shown in Figure 27, with important components identified. The board has been successfully tested and is operational.

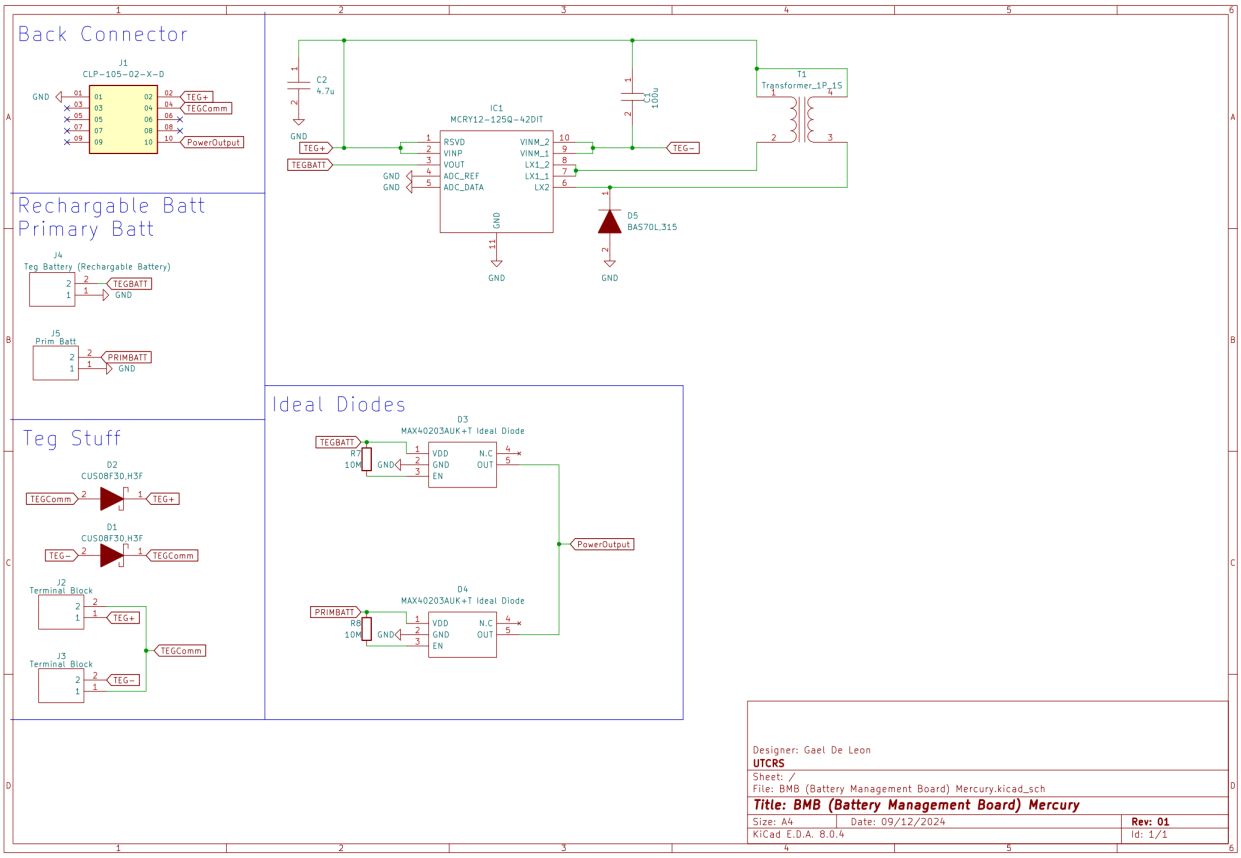

Figure 28: Schematic of battery management board (Mercury version)

(Note: This high-resolution image can be zoomed for enhanced detail)

6.3 Battery management board – Mercury version circuit

The schematic for the Mercury version of the battery management board is shown in Figure 28. It has a lower parts count and relies on transformer T1 to enable cold start from very low voltages (as low as 25mV), while tolerating inputs as high as 7V. The primary drawback is that IC1, the MCRY12-125Q-42DIT boost converter, has a maximum output current of 4mA.

Diodes D1, D2, D3 and D4 have the same functions as in the E-Peas version of the circuit. Please refer to Section 6.1 for a description of their functions. The connectors also have similar functions but are repeated here for reference:

Connector J1 supplies power and monitoring lines to the mainboard. Pins 1 (GND) and 10 (Power Output) are the power to the main board, drawn either from the storage device or the backup primary battery. When operating properly (i.e., either the primary or secondary battery has

sufficient charge), the board should output between 3.35V and 4.2V. The lower limit is set by the dropout voltage for the regulators on the mainboard, while the upper limit is set by the maximum safe voltage for a single cell lithium-ion battery. The other connected pins (2 and 4) can be used to directly monitor the energy harvesting sources.

Connectors J2 and J3 and for two TEGs operated in series. In cases where there is a single harvesting device, for example, a single TEG or a solar cell, it should be connected with the negative terminal to Pin 2 on J3 and the positive terminal to Pin 1 on J2, with the other pins left unconnected.

Connectors J4 and J5 are for the storage device (TEGBATT) and primary battery, respectively.

6.4 Battery management board – Mercury version PCB, fabrication, and status

The PCB layout for the Mercury version of the battery management board is shown in Figure 29. The board measures 31.8×30.7mm, has four copper layers, and is on FR-4 substrate with a total thickness of 1.6 mm. An annotated photograph of the blank PCB is shown in Figure 30. As of the date of the report, the Mercury version was still in assembly and had not yet been tested.

A bill of materials and links to obtain CAD files are given in the Appendix.

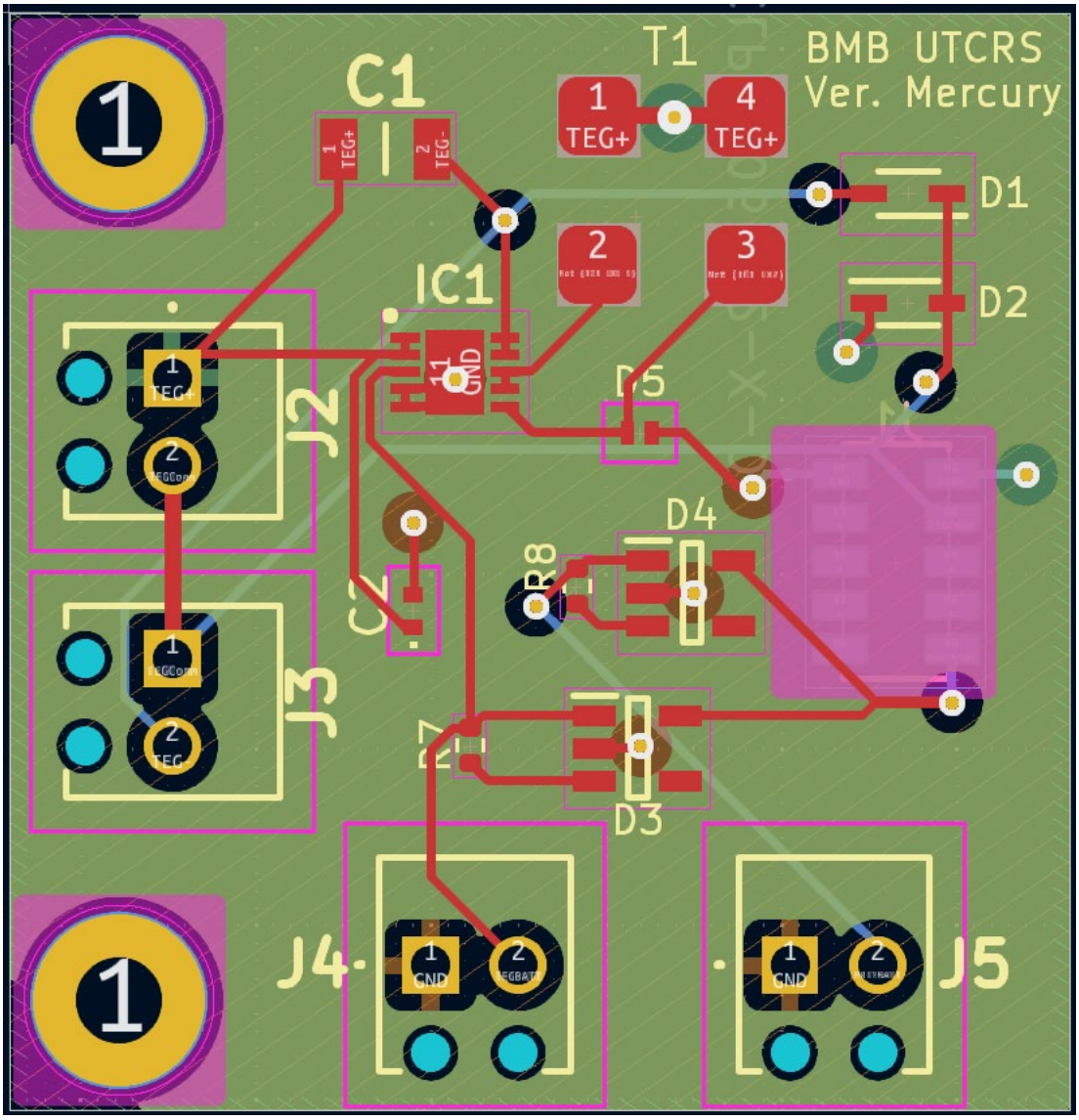

Figure 29: Battery management board PCB layout (Mercury version)

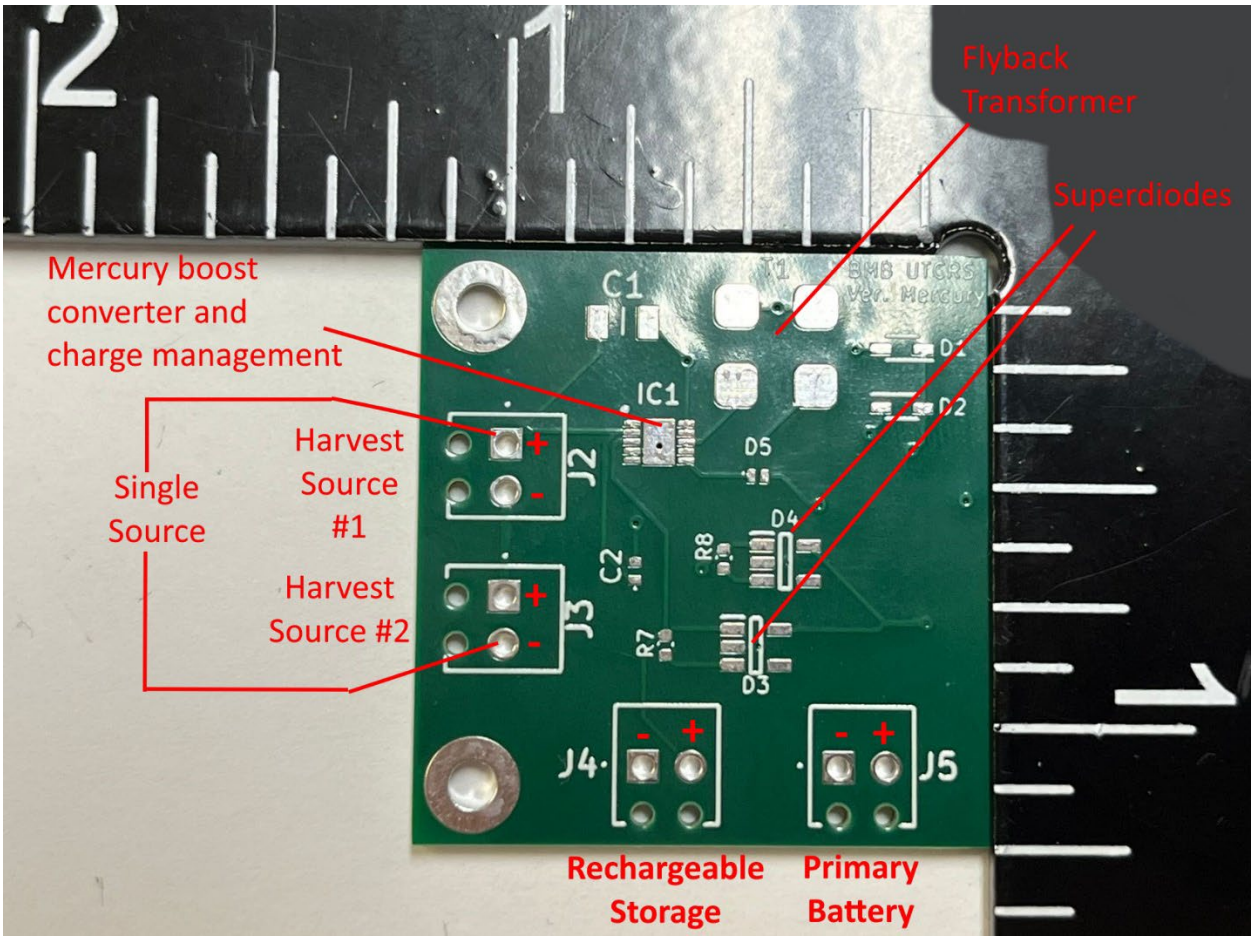

Figure 30: Blank PCB for battery management board (Mercury version)

7 Wired Data Acquisition Alternative

7.1 Wired DAQ overview and specifications

While the primary objective of this project is *wireless* onboard sensors, there are situations in a test environment where it is useful to have the certainty and simplicity of a wired connection. The wired data acquisition (DAQ) board described here allows testing of methodologies like synchronized sampling on up to eight separate analog accelerometers while the wireless testbed described in the previous chapters is under development. It includes filtering equivalent to current generation wireless sensors, ADC resolution enhanced to 16 bits, eight separate ADCs with synchronized clocks and conversion triggers, and SRAM storage on the PCB. Serial (UART) communications allow the board to be controlled from, and data downloaded to, a variety of platforms. The board is compact and capable of battery operation, making it suitable for field use on test tracks, where temporary wiring harnesses under the railcar may be acceptable. A summary of the specifications is given in Table 2 below.

Table 2: Wired DAQ Board Specifications

Category	Requirement
Analog Channels	8 single-ended channels. Input range 0V -5V. Simultaneous operation.
Input Connectors	Option 1: For accelerometer modules with UTCRS tester standard pinout: 1.5mm pitch, 8 pin Click-Mate connectors, two channels per connector, pinout includes power for accelerometers and self-test control. Option 2: For generic data acquisition: Standard 2.54mm dual row male header, one signal/ground pair per channel.
Filtering	8^{th} order elliptic switched capacitor filter in each channel. Cutoff frequency matched and determined by a single clock. Cutoff frequency tunable 600 Hz to 6 kHz with onboard clock. External clock can be used (jumper selection). Filters can be bypassed (jumper selection).
ADC Conversion	Separate ADC for each channel. Synchronized trigger and conversion clock across all channels. 16-bit resolution SAR. Single voltage reference for all channels.
Sampling	Sample rate and shot length programmable via serial port. >50 ksamps/sec. Maximum shot 32768 samples × 8 channels
Data Storage	Static random-access memory.

	32768 samples x 8 channels x 2 bytes/sample.
Communications	TTL level (5V) serial UART. 115000 baud, 8 bits, 1 stop, no parity.
Power Supply	External supply required: 6 to 7.5V DC, 1A. Draws <100mA average while active.
Dimensions	5.0"×5.0" (127mm×127mm)

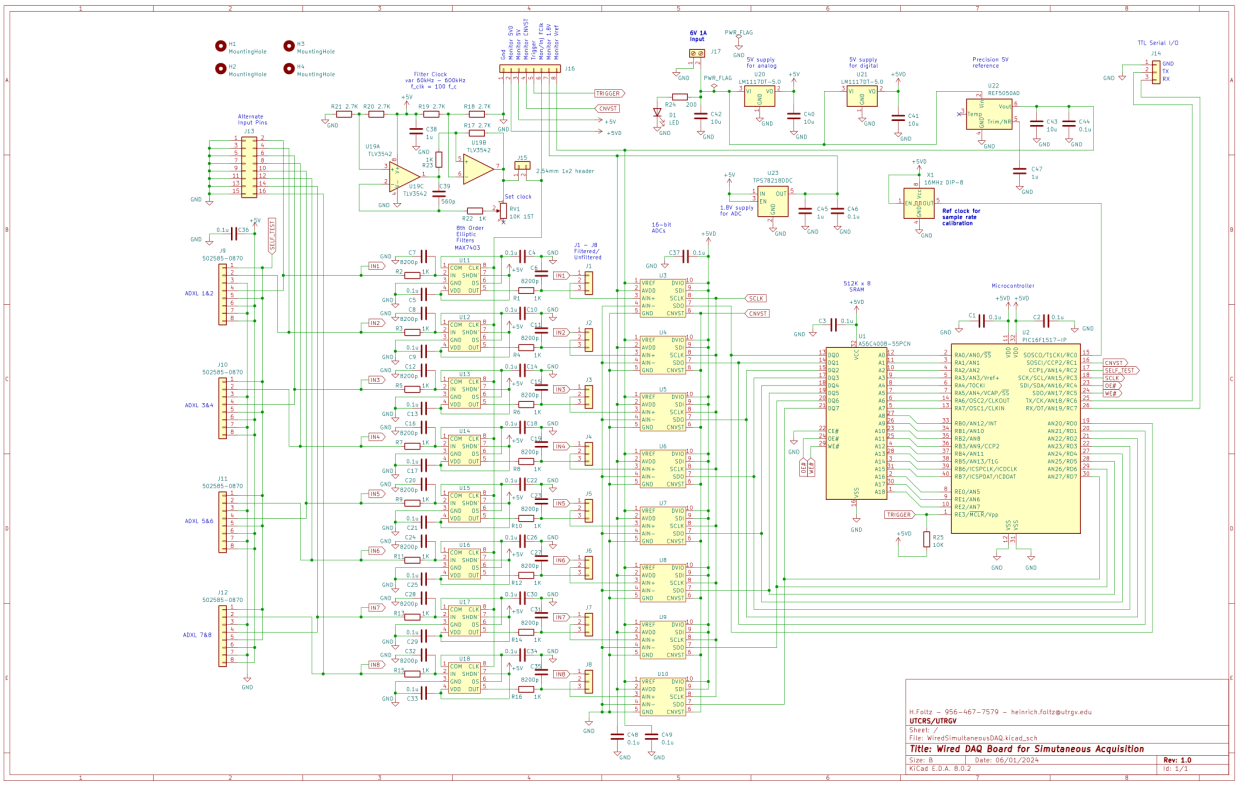

Figure 31: Wired DAQ board for simultaneous acquisition.

(Note: This high-resolution image can be zoomed to show more detail)

7.2 Wired DAQ circuit

The overall circuit for the wired DAQ board is shown in Figure 31. The key elements are (a) a bank of eight switched capacitor filters to condition the accelerometer signals, (b) a bank of eight successive approximation analog-to-digital converters (ADCs) with serial outputs, (c) a static random-access memory (SRAM) that stores the data streams from the ADCs, and (d) a microcontroller unit that manages the start time for shots, the sample rate, and the shot length, as

well as responding to user commands and data requests made through the serial communication port.

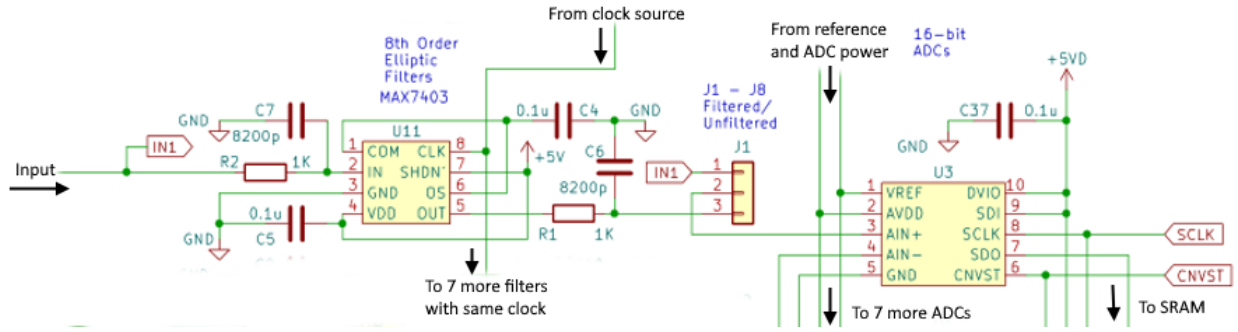

Figure 32: Wired DAQ board detail: Single channel

(This detail shows one of eight input channels on the board)

7.3 Wired DAQ signal conditioning and conversion

Figure 32 shows the signal path for a single channel. U11 is a MAX7403 switched capacitor filter, 8th order, elliptic characteristic with transition ratio $r = 1.2$. The cutoff frequency is set by the clock input on pin 8; the clock is common to all filters to ensure identically matched characteristics. The cutoff given by $f_{co} = f_{clk} / 100$, where f_{co} is the cutoff frequency and f_{clk} is the clock frequency. R1 and C7 on the input side of the filter are to reduce aliasing of signals above the clock frequency, while R1 and C5 are to reduce clock signal leakage from the output.

Jumper J1 chooses whether the analog-to-digital converter, U3, reads from the input (unfiltered) side or output (filtered) side of the filtering section. The ADC itself is an MCP33131-05 by Microchip. It is a single-channel, 16-bit, successive approximation (SAR) converter with serial output. Although it is SPI compatible, it does not in fact use the data input pin (SDI = MOSI) which is tied high in this circuit. The conversion start pin (CNVST) has the function of both conversion trigger and chip enable on a normal SPI interface: when it is taken high the chip acquiring the input analog voltage and begins conversion, when it is brought low after a suitable delay to allow the conversion to complete, the 16-bit can be read sequentially from the output (SDO = MISO) using the SCLK to clock out the data.

Each channel has one ADC; all eight are tied to the same CNVST and SCLK line generated by the microcontroller to ensure synchronous operation. The outputs are separately routed, each to one

of data lines DQ0 through DQ7 of the SRAM, as shown in Figure 33 and described in the next section.

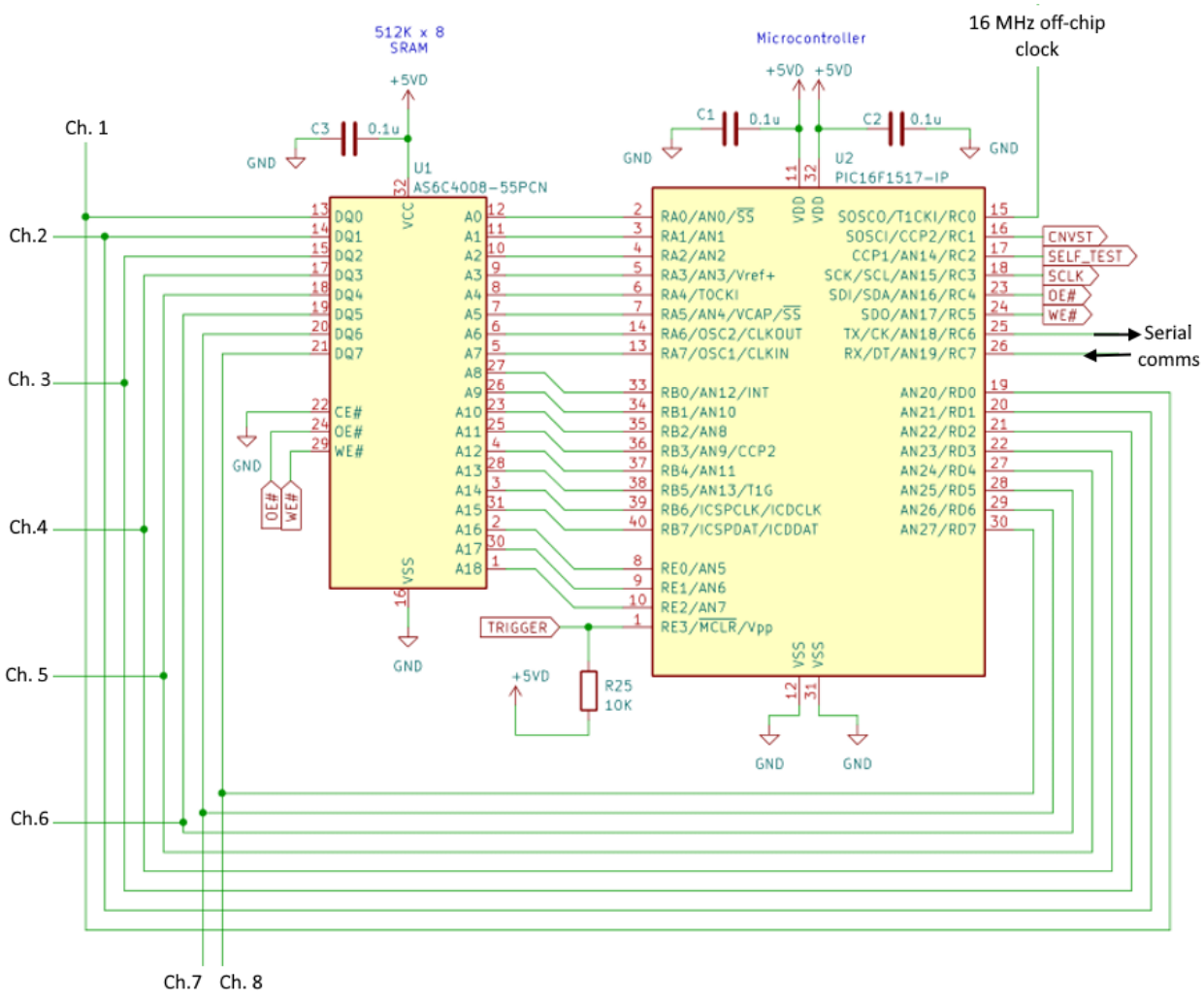

Figure 33: Wired DAQ board detail: SRAM and MCU

7.4 Wired DAQ SRAM and MCU

Referring to Figure 33, the SRAM U1 is an AS6C4008-55PCN by Alliance Memory, organized as 524,288 words × 8 bits/word. Its data lines are bidirectional and connected to both the output lines of the ADCs (to store sample data during a shot) and to the MCU (to retrieve data after a shot is complete). The microcontroller U2 is a PIC16F1517 by Microchip. Port A (RA0-RA7), Port B (RB0-RB7) and all but one pin of Port E (RE0-RE2) are configured as outputs and used to set the SRAM address pins A0-A18. Port D (RD0-RD7) is mapped directly to the SRAM data lines DQ0-

DQ7. Port C is used for clock, control, and communication signals, including the CNVST signal that initiates conversion, the SCLK signal used to clock data out of the ADCs and into the SRAM, the OE# and WE# lines used to control whether the SRAM is in read or write mode, and the receive and transmit pins for the UART communications.

It should be noted that all I/O pins on the MCU are used and there is no provision for in-circuit programming. The MCU is a socketed device in a 40-pin dual inline package and is flashed while out of the circuit in a programming fixture.

7.5 Data acquisition sequence and data storage format

The MCU uses the following sequence to store a shot of N samples at sample rate f_{samp}:

(1) Ensure that MCU lines RD0-RD7 are high-impedance (configured as inputs), so that ADCs can control the data lines.
(2) Initialize memory address A0-A18 to a starting point (typically 0x00000).
(3) Set up MCU timer to rollover at intervals of $1/f_{samp}$ by setting the preset and pre-scaler values.
(4) Enable timer interrupts.
(5) Respond to each interrupt as follows:
    (a) Take CNVST high to initiate conversion.
    (b) Wait ~1 μsec to ensure completion.
    (c) Take CNVST low to begin reading data.
    (d) Repeat 16 times (from MSB to LSB of converted results):
        i. Pulse WE# active to read one bit from each ADC into a memory word.
        ii. Pulse SCLK active to cause ADCs to output next most significant bit.
        iii. Increment memory address.
    (e) Increment sample count.
    (f) If sample count reaches N, disable timer interrupts.
(6) Take CNVST high and leave high so that the ADCs release the data lines to high-impedance, allowing use by the MCU.

After the sequence is completed, the data will be stored in SRAM as shown in Figure 34. Note that each 8-bit memory location contains one bit of data from each of eight channels; therefore, sixteen locations must be read to get one sample point, even if only one channel is of interest.

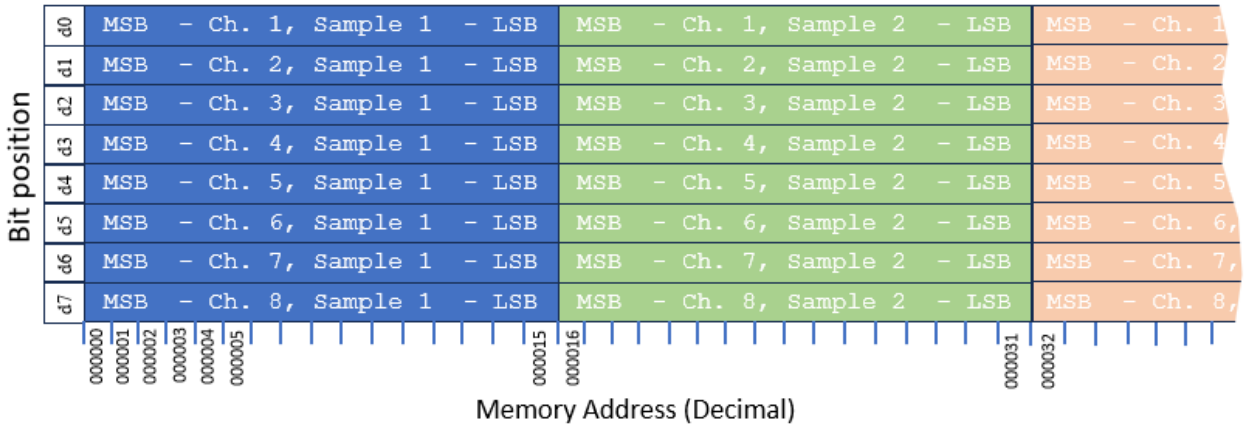

Figure 34: Wired DAQ data storage in SRAM

7.6 Wired DAQ filter clock

The switched capacitor filters described in Section 7.3 require a clock to operate. The filter clock generator shown in Figure 35 uses a standard triangular-square wave circuit consisting of a Miller integrator followed by hysteresis circuit in a feedback loop; both stages have their reference inputs set at 2.5V rather than ground to allow single supply operation. A ten-turn trimmer potentiometer RV1 is used to set the clock frequency f_{clk} to 100 times the desired cutoff frequency f_{co} for the switched capacitor filters. During the adjustment, f_{clk} can be observed using an oscilloscope or frequency counter attached to the clock monitor pin (J16 pin 6).

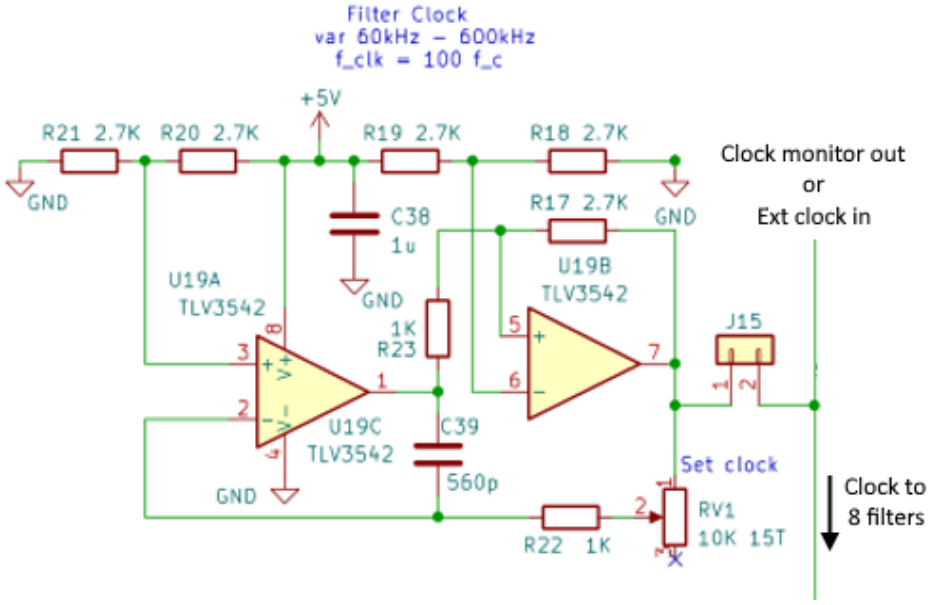

Figure 35: Wired DAQ board detail: Filter clock generator

7.7 Wired DAQ voltage regulation and sampling clock

The voltage regulation and MCU clock sections of the circuit are shown in Figure 36. The main power input at J17 is nominally 6V but should tolerate any DC source in the range 6.0-7.5V. It does not need to be accurately regulated, and any of the following power sources should be adequate: unregulated 6V supply, a series pack of four standard 1.5V alkaline cells, or a 7.5V lithium battery pack.

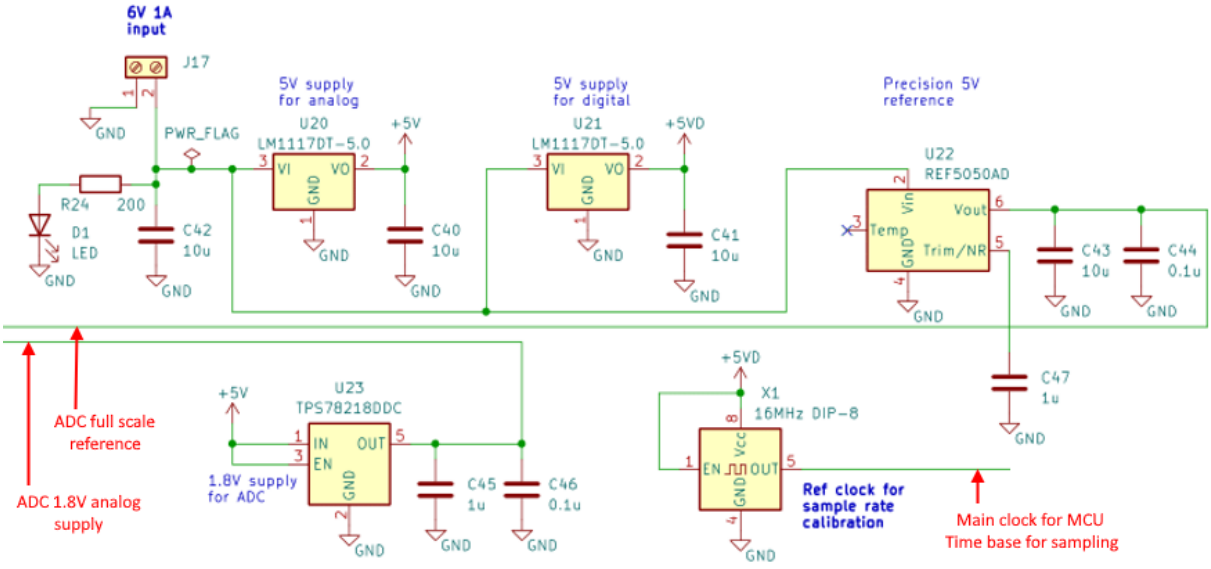

Figure 36: Wired DAQ board detail: Voltage regulation and sampling clock

Separate 5V LDO regulators are used for the analog (U20) and digital (U21) portions of the circuit. A separate precision voltage source (U22, an REF5050AID from Texas Instruments with 0.1% initial accuracy and 3ppm/°C temperature coefficient) is used to provide an accurate and stable full-scale reference for the ADCs. The ADCs also need a separate 1.8V supply which is provided by U23.

Finally, X1 is a 16 MHz clock module that is connected to the external clock input (T1CK1/RC0) for the internal MCU timer (TIMER1) that generates the sample interrupts. The MCU has a selectable pre-scaler that can divide the 16 MHz by a factor of 1, 2, 4, or 8. When active, the timer counts up to a 16-bit preset value, at which point an interrupt is generated (which initiates an ADC conversion) and the timer resets. Thus, the longest possible period between samples using this method is 65535 × 8 / 16 MHz = 32.7675ms, so that the slowest available sample rate is 30.5 Hz.

More realistically, for bearing monitoring, a preset of 3077 with a pre-scale factor of 1 would be typical. These values lead to a period of 3077 × 1 / 16 MHz = 192.3µs, for a sample rate of 5.1998 kHz.

7.8 Wired DAQ board PCB and fabrication

The PCB layout for the wired DAQ is shown in Figure 37. Since this board is not intended to be mounted directly on a bearing adapter, but instead mounted to the underside of the railcar, it was not necessary to miniaturize. The board is 5.0in×5.0in (127mm×127mm) in size, four layers, and is on an FR-4 substrate with a total thickness of 1.6mm. An assembled version with major sections labeled is shown in Figure 38.

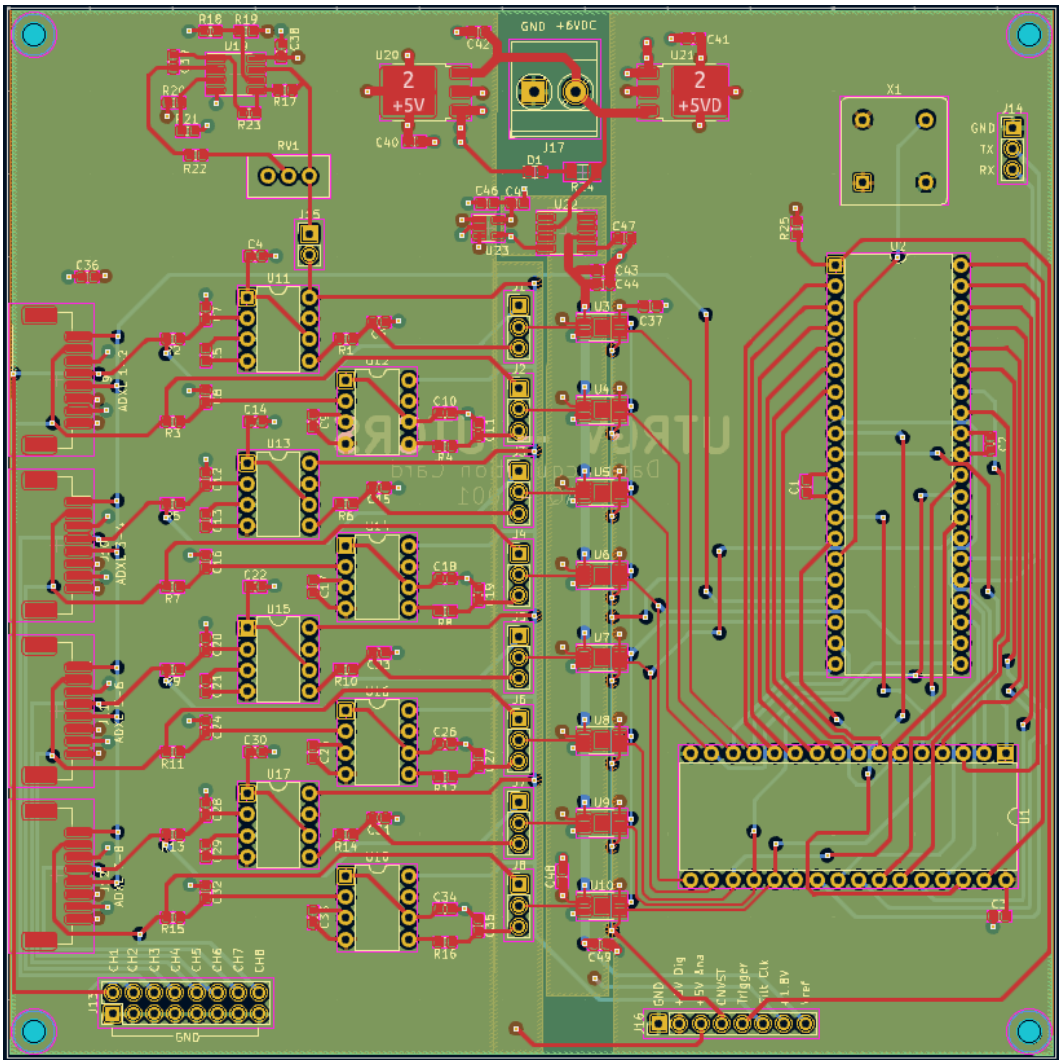

Figure 37: Wired DAQ board PCB layout (Revision 1 shown)

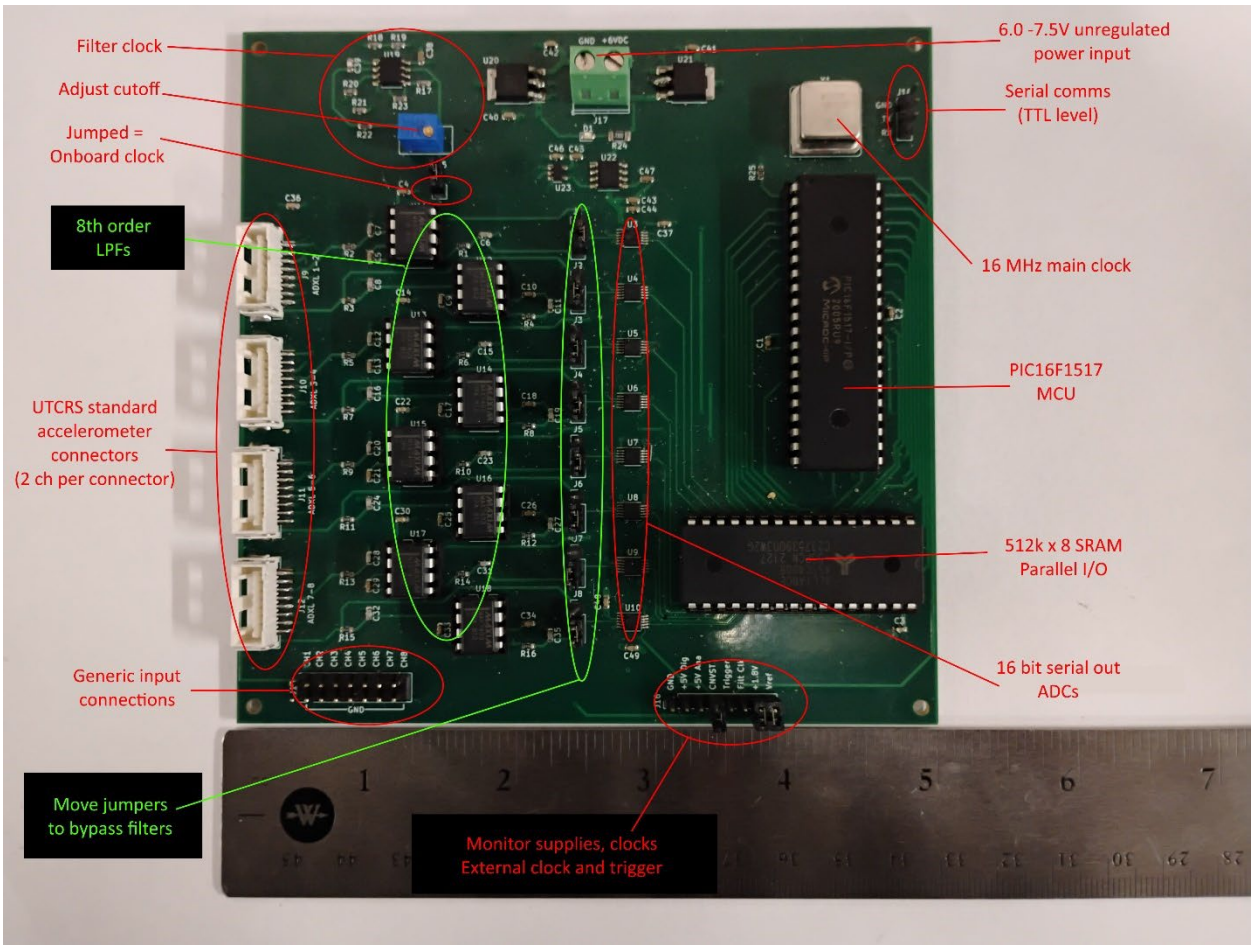

Figure 38: Fabricated wired DAQ board (annotated, Revision 1 shown)

7.9 Wired DAQ board status

The figures in the preceding sections were for Revision 1 of the board, which has been assembled and tested. A functional beta version of the PIC16 firmware has been completed, along with a Windows application (Figure 39) that can connect to the wired DAQ using an off-the-shelf USB-to-TTL Serial adapter. A combined system of accelerometers, wired DAQ board, firmware, and Windows application was tested over more than 72 hours on a running bearing test rig in the UTCRS laboratories. The system obtained vibration data that was validated against existing systems (National Instruments DAQ with LabView software). As of the date of the report, these parts of the system are judged to be ready for field testing by the project personnel.

A bill of materials and links to obtain CAD files are given in the Appendix.

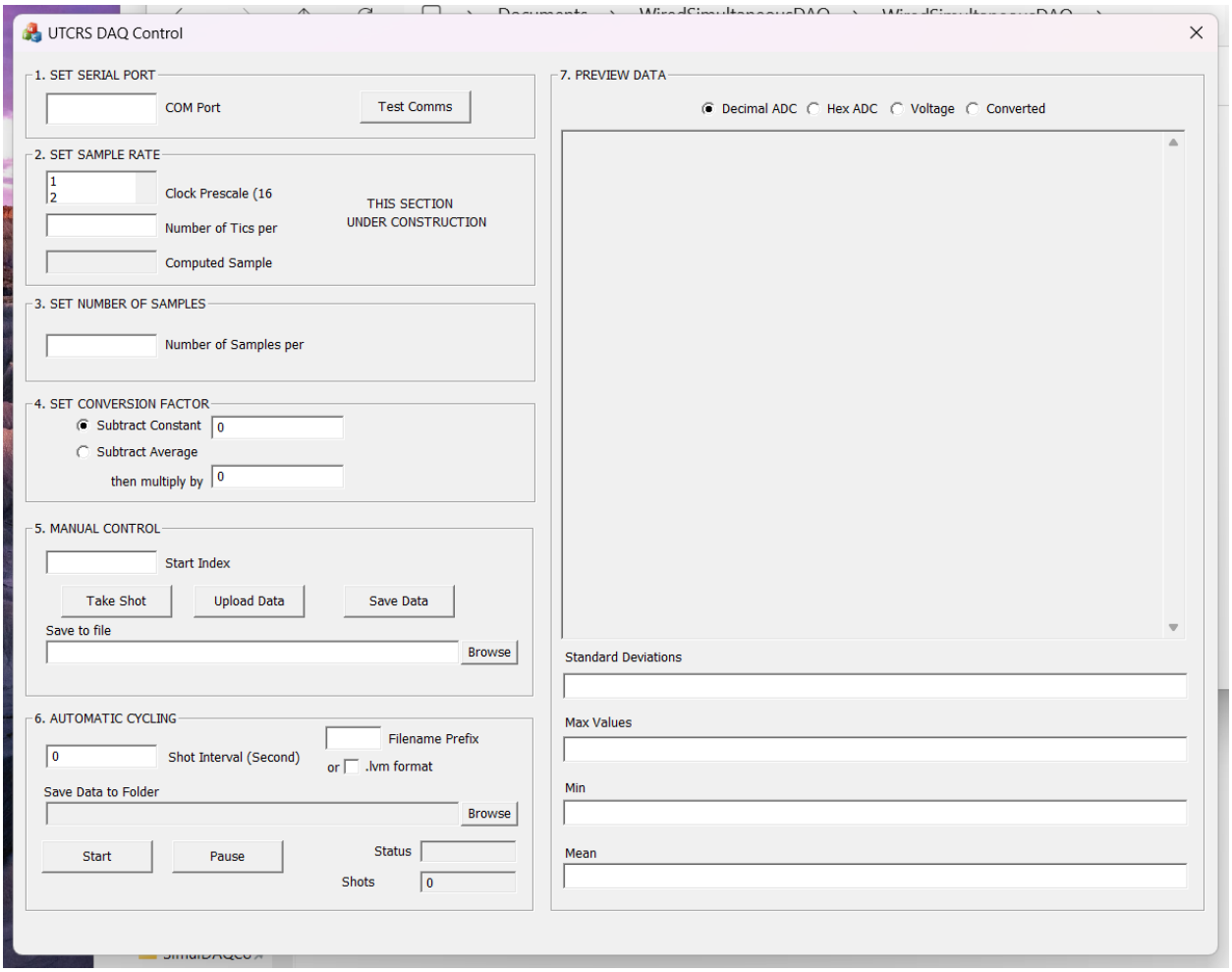

Figure 39: Screenshot of Windows application for use with wired DAQ

8 Conclusions and Future Work

8.1 Summary of Completed Work

The purpose of this project was to develop a new, compact, and flexible wireless module for onboard monitoring of bearing and wheel condition, with possible future extensions to track and coupling conditions, that would serve as a testbed for evaluation of new techniques for data sampling, data processing, power management, energy harvesting, and communications systems. This system will facilitate fusion of data from multiple bearings and wheels on a car, research into new techniques for power reduction and battery life extension, and comparative studies of different communication frequency bands and protocols. Primary accomplishments for this project were:

(a) Development of system requirements and specifications.

(b) Hardware design and fabrication for a sensor mainboard.

(c) Hardware design and fabrication for a 900 MHz LoRa communications daughterboard.

(d) Hardware design and fabrication for a 2.4 GHz communications daughterboard.

(e) Hardware design and fabrication for one battery management daughterboard.

(f) Hardware design for a second battery management daughterboard.

An additional project was completion and testing of hardware, firmware, and user software for a portable wired system that can be used to field test new sampling and data processing techniques for improved noise reduction and identification of impact sources.

8.2 Future Work

The next phase will require completion of firmware for the mainboard and two communications boards. A minimum starter package must include firmware modules to (a) synchronize clocks based on broadcasted timing packets, (b) acquire vibration and temperature data at precise start times and sample rates, (c) process data to reduce noise, compute statistics, and apply defect detection algorithms, and (d) respond to requests for data received via wireless. In parallel, the completed wired system can be used both in the lab and in the field (on test tracks) to determine the magnitude of crosstalk, evaluate new methods for identifying the sources of single-impact events, and cross-validate data against both commercial onboard sensors and wayside detectors.

9 References

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[2] M. Barrera, L. Cantu, C. Tarawneh, H. Foltz, B. Wilson, and B. Porter, "Pilot Field Test of an Onboard Wireless Health Monitoring System for Railroad Rolling Stock," ASME Joint Rail Conference, Online, Virtual, April 20-21, 2022.

[3] L. Villafranca, M. Noruzoliaee, C. Tarawneh, and A. Sanchez-Trinidad, "Predicting the Remaining Service Life of Railroad Bearings: Leveraging Machine Learning and Onboard Sensor Data," ASME Joint Rail Conference, Online, Virtual, April 20-21, 2022.

[4] C. Tarawneh, J. Montalvo, and B. Wilson. Defect detection in freight railcar tapered-roller bearings using vibration techniques. Railway Engineering Science, 29(1): 42-58, 2021. https://doi.org/10.1007/s40534-020-00230-x

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[7] Cantu, L. R. (2021). Assessing the Effectiveness and Efficacy of Wireless Onboard Condition Monitoring Modules in Identifying Defects in Railroad Rolling Stock. Edinburg, TX, United States: Master's Thesis. The University of Texas Rio Grande Valley.

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[10] Siddiqui, F.M. and Maurya, V.K., "Study of TEG When Connected in Series and Parallel Combinations Along With a DC-DC Converter," *Vivechan International Journal of Research*, Vol. 8, Issue 1, 2017.

10 Appendix

10.1 Bill of materials

The following tables contain bills of materials for the hardware modules described in this report. Inclusion of part numbers and names of particular distributors and manufacturers is for documentation purposes and should not be interpreted as endorsement of a specific sources. With the exception of a few special purpose integrated circuits, most of the parts are generic and can be exchanged with any other part sharing the same package and description.

Table 3: Bill of materials for main sensor board

Part Number	Schematic Reference	Qty	Description
04023D105KAT2A	C1, C15, C29, C31	7	1µF capacitor 0402
0402ZD106MAT2A	C13, C24	2	10µF capacitor 0402
VJ0402Y472KXAAC	C17	1	4.7nF capacitor 0402
04025C104KAT4A	C2, C3, C4, C5, C6, C7, C11, C16, C18, C20, C23, C28, C30	13	0.1µF capacitor 0402
C0402C109D5GACTU	C26, C27	2	1pF capacitor 0402
CC0402JRNPO9BN161	C6	1	160pF capacitor 0402
C0402C809B5GACTU	C9, C10	2	8pF capacitor 0402
SML-LX0402GC-TR	D1	1	Green LED 0402
SML-LX0402SIC-TR	D2	1	Red LED 0402
BLM31KN601SH1L	FB1	1	600 ohm Ferrite bead
PIC32CM3532LE00064-I_PT	IC1	1	ARM®Cortex®M23 PIC®32CM Microcontroller IC 32-Bit 48MHz 512KB (256Kx 16) FLASH 64-TQFP (10x10
TPS78233DDCT	IC2, IC5, IC8	4	3.3V Voltage Regulator
ADS8344E	IC4	1	8 channel 16-bit Analog to Digital Converter 100kS/s
REF196GSZ-REEL	IC6	1	3.3V Voltage Reference
INA333AIDGKT	IC7	1	Instrumentation Amplifier
KXI34ACR-LBZE2	IC9	1	Rohm Kionix®64g three axis accelerometer
CLP-104-02-F-DH-TR	J1	1	8 pin connector for load cell female
M50-3600542	J2, J3, J4	3	Dual row 0.05” header 2 x 5

MLF1608E100KTD00	L1	1	10 µH inductor 0603
CRT0402-FZ-1502GLF	R1, R7	2	15kΩ Resistor 0402
WF04H1004DTL	R10, R11, R12, R13, R14, R15	6	1MΩ Resistor 0402
NCP15WF104F03RC	R2	1	100kΩ Resistor 0402
ERJ-2RHD221X	R3, R9	2	220Ω Resistor 0402
CR0402-FX-2002GLF	R4, R5	2	20kΩ Resistor 0402
RT0603BRD07626RL	R6	1	626Ω Resistor 0.1% tolerance
NT0402BRD071KL	R8	1	1k ohm 0.1% precision resistor 0402
NB-PTCO-050	TH1	1	PTC Thermistor
ADXL1001BCPZ	U1	1	Single axis analog accelerometer
MAX7407CSA+	U2	1	8th order elliptic filter
LMT84DCKR	U3	1	Temperature Sensor IC
ECX-.327-CDX-2096	Y1	1	32.768KHz Crystal C_{load} = 12.5pF
ABM10W-32.0000MHZ-6-B1U-T3	Y2	1	32MHz Crystal C_{load} = 6pF

Table 4: Bill of materials for communications board (LoRa)

Part Number	Schematic Reference	Qty	Description
81-GRM155R71A104KA1J	C1, C2, C3	3	0.1 uF 10 VDC 10% X7R 0402
810-C1005X5R0J475KE	C4, C9	2	6.3V 4.70uF X5R 10% 0402
81-GRM155Z71A105KE1J	C5	1	1 uF 10 VDC 10% X7R 0402
77-VJ0402Y103KXQCBC	C6	1	0402 0.01uF 10volts X7R 10% 0402
81-GRM0335C1H680FA1D	C7, C8, C17, C21	4	68 pF 50 VDC 1% 0201
81-GRM155R61A474KE5D	C10	1	0.47 uF 10 VDC 10% 0402
710-885012005006	C11, C12	2	6.8pF 0.5pF 10V 0402
81-GJM0335C1E120FB1D	C13, C14	2	12 pF 25 VDC 1% 0201
81-GRM0335C1E12FA1D	C15, C16	2	1000 pF 25 VDC 1% 0201
81-GJM0335C1H3R3WB1D	C18, C19	2	3.3 pF 50 VDC 0.05 pF 0201
81-GRM033R60J473JE9D	C20	1	0.047 uF 6.3 VDC 5% 0201
511-BALFHB-WL-03D3	IC1	1	Signal Conditioning Integrated filter matched balun to QFN STM32WL high power, 862-928 MHz, 2 layer
855-M50-3600542R	J1	1	Headers & Wire Housings ArcherM50 1.27mmPitc DIL Vert Pin Head
712-CONMHF1-SMD-T	J2	1	Coaxial Connector MHF1 Connector Receptacle, Male Pin 50 Ohm Surface Mount

200-CLP10502FD	J3	1	Low Profile Dual-Wipe Socket, .050" Pitch
81-LQM18DN150M70L	L1	1	15uH 20% 220mA SMD 0603
810-MHQ0603P9N1HT000	L2	1	9.1nH S-HQ SMD 0201
581-LCCI0201J33NGTAR	L3	1	33nH Tol 5% 0201 120mA DCR=2.1 Ohms
603-RC0201JR-7D0RL	R1, R2	2	0 Ohms 50mW 0201 5%
603-AC0201FR-07100RL	R3, R4	2	100 Ohms 50 mW 0201 1%
726-BGS12WN6E6327XTS	U2	1	RF Switch IC
511-STM32WL55CCU7	U3	1	RF Microcontroller - MCU Multiprotocol LPWAN 32-bit ArmCortex-M4 MCUs LoRa (G)FSK-MSK BPSK 256KB Flas
428-202257-MC01	Y1	1	Crystal 32.768 kHz 12.5 pF +/-20 PPM -40/+85C
732-FA-12832MF20X-K5	Y2	1	Crystal 32 MHZ +/-10PPM +/-20PPM -40~85C 10PF 3KTR

Table 5: Bill of materials for communications board (2.4 GHz)

Part Number	Schematic Reference	Qty	Description
nRF52840-QFAA-F-R7	U1	1	RF System on a Chip - SoC Multiprotocol Bluetooth 5.3 SoC supporting Bluetooth Low Energy, Bluetooth mesh, NFC, Thread and Zigbee
CONMHF1-SMD-T	J3	1	MHF1 Connector Receptacle, Male Pin 50 Ohm Surface Mount Solder
CLP-105-02-F-D	J2	1	Low Profile Dual-Wipe Socket, .050" Pitch
M50-3600542	J1	1	Header 5+5 DIL PIN HDR SMT Au/Sn
830066198	X2	1	Crystals WE-XTAL 32.7680kHz 20ppm 1.6 x 1.0mm
830108212909	X1	1	Crystals WE-XTAL 32.0MHz 15ppm 2.0 x 1.6mm
GRM0335C1E120GA01D	C1, C2, C16, C17	4	12 pF 25 VDC 2% 0201 C0G (NP0)
MBASU063SCG010BFNA01	C3	1	50V 1pF C0G 0201 0.6x0.3x0.3mm -55+125C Tol=0.1pF

MBASU063SCG1R2BFNA01	C4	1	50V 1.2pF C0G 0201 0.6x0.3x0.3mm -55+125C Tol=0.1pF
C0603X5R1A104K030BC	C5, C6, C7, C8, C12	5	0201 10VDC 0.1uF 10% X5R 0.3mm
0201YA101JAT2A	C11	1	16V 100pF C0G 0201 5 % A581-0201YA101JAT4A
KGM05AR50J105KH	C13, C14	2	6.3V 1uF X5R 0402 10 %
MSASE063SB5473KFNA01	C15	1	16V 0.047uF X5R 0201 10 %
CBMF1608T100K	L3	1	0603 10uH 468mOhms 10% 115mA
7447820047G	L1	1	WE-MK 0.28A 4.7nH 0201 DCR=300 mΩ
7447820022G	L2	1	WE-MK 0.36A 2.2nH 0201 DCR=190 mΩ
744784115A	L4	1	WE-MK Multilayer Ceramic SMT Inductor 15nH 0402

Table 6: Bill of materials for battery management board (E-Peas version)

Part Number (Mouser)	Schematic Reference	Qty	Description
81-GRM155R61A106ME1D	C1	1	10 uF 10 VDC 20% 0402 X5R
346-CM05X5R226M6AH80	C2	1	22 uF 10 VDC 20% 0603 X5R
81-GRM188R61A226ME5J	C3, C4	2	22 uF 10 VDC 20% 0603 X5R
757-CUS08F30H3F	D1, D2	2	Schottky Diode, 30V, 800mA, USC
700-MAX40203AUK+T	D3, D4	2	Ideal diode current switch, SOT-23
120-AEM20940-QFN	IC1	1	Thermal Energy Harvesting Manager QFN-28
200-CLP10502FD	J1	1	Dual row 0.05" female header 2x5
651-1725656	J2, J3, J4, J5	2	Fixed Terminal Blocks 2P 2.54mm 90DEG
810-MLZ1608M100WT000	L1, L2	1	10uH 20% 1608
71-RCC0402100RFKED	R1, R2, R3, R4, R5, R6	6	1/8W 100ohms 1% 100ppm 0402
603-AC0402FR-0710ML	R7, R8	2	10 MOhms 62.5mW 0402 1%

Table 7: Bill of materials for battery management board (Mercury version)

Part Number (Mouser)	Schematic	Qty	Description

	Reference		
963-JMK316BJ107ML-T	C1	1	6.3V100uF X5R 1206 20 %
81-GRM155R60J475ME8J	C2	1	4.7 uF 6.3 VDC 20% 0402 X5R
757-CUS08F30H3F	D1, D2	2	Schottky Diode, 30V, 800mA, USC
700-MAX40203AUK+T	D3, D4	2	Ideal diode current switch, SOT-23
771-BAS70L315	D5	1	Schottky Diode, 70V, 70mA, SOD882
411-MCRY12-125Q42DIT	IC1	1	Energy Harvesting Synchronous Boost Converter with Microwatt Cold-Start, Input Impedance Matching and Regulated Output DFN-10
200-CLP10502FD	J1	1	Dual row 0.05" female header 2x5
651-1725656	J2, J3, J4, J5	4	Fixed Terminal Blocks 2P 2.54mm 90DEG
603-AC0402FR-0710ML	R7, R8	2	10 MOhms 62.5mW 0402 1%
994-LPR6235-123QMRC	T1	1	Coupled Inductors 12.5uH 12% 900mA 200 Ohms

Table 8: Bill of materials for wired DAQ board

Part Number (Mouser)	Schematic Reference	Qty	Description
80-C0603C104K4R	C1-C5, C9, C10, C13, C14, C17, C18, C21, C22, C25, C26, C29, C30, C33, C34, C36, C37, C44, C46, C48, C49	25	KEMET 16V 0.1uF X7R
81-GRM1885C1H822JA1J	C6-C8, C11, C12, C15, C16, C19, C20, C23, C24, C27, C28, C31, C32, C35	16	Murata Electronics 8200 pF 50 VDC 5% C0G 0603
187-CL10A105KA8NNNC	C38, C45, C47	3	Samsung Electro-Mechanics 1uF+/-10% 25V X5R 0603
80-C0603C561J5GAC	C39	1	KEMET 50V 560pF C0G 0603
81-GRM188R61A106ME9D	C40-C43	4	Murata Electronics 10 uF 10 VDC 20% 0603

604-APT1608ZGC-AMT	D1	1	Kingbright 1.6x0.8mm Green Standard 0603
649-78511-403HLF	J1-J8, J14	9	1x3 pin 2.54mm vertical male header, unshrouded
538-502584-0860	J9-J12	4	8 pin 1.5mm Clik-Mate receptacle, vertical surface mount
649-1012938191601BLF	J13	1	2x8 pin 2.54mm vertical male header, unshrouded
649-78511-402HLF	J15	1	1x2 pin 2.54mm vertical male header, unshrouded
649-1012937890801BLF	J16	1	1x8 pin 2.54mm vertical male header, unshrouded
651-1729128	J17	1	Terminal block, 2 position, 5.08mm
603-RT0603FRE071KL	R1-R16, R22, R23	18	YAGEO 1Kohm 1% 1/10W 0603
603-RC0603FR-072K7P	R17-R21	5	YAGEO 2.7kOhms 1% 1/10W 0603
603-RC1206FR-7W200RL	R24	1	YAGEO 200 Ohms 1% 500 mW 1206
652-CRT0603FZ1002ELF	R25	1	Bourns 10K1% 1/10W 0603
652-3296W-1-103R	RV1	1	10K25T trimmer, top adjust, Bourns 3296X series
913-AS6C4008-55PCN	U1	1	AS6C4008-55PCN – Alliance Memory - SRAM 4M, 2.7-5.5V, 55ns 512Kx8 Asynchronous DIP32 (socketed)
579-PIC16F1517-I/P	U2	1	PIC16F1517-IP – Microchip Technology - MCU 14KB Flash 512B RAM 1.8-5.5V DIP40 (socketed)
579-MCP33131-10-E/MS	U3-U10	8	MCP33131 - Microchip Technology - ADC 16-bit, 1 Msps, single channel, single-ended SAR, MSOP-10
700-MAX7403CPA	U11-U18	8	MAX7403CPA+ - Analog Devices – 8th order elliptic switched capacitor LPF, DIP8 (socketed)
595-TLV3542IDR	U19	1	TLV3542IDR – Texas Instruments – Dual R-to-R Op Amp 200 MHz, SOIC-8
926-LM1117DTX50NOPB	U20, U21	2	LM1117DTX-5.0/NOPB – Texas Instruments 5V 800mA LDO regulator, TO-252-3

595-REF5050AIDR	U22	1	REF5050AIDR – Texas Instruments - precision 5.0Vreference, SOIC-8
595-TPS78218DDCR	U23	1	TPS78218DDCR Texas Instruments – 1.8V150mALDO regulator, SOT-23-5
774-MXO45HST-3C-16.0	XI	1	Oscillator - CTS Electronic Components 16MHz 50ppm 8Pin DIP

10.2 CAD and firmware files

Current CAD files for all the boards mentioned in this report, as well as firmware and application software for the wired DAQ board, are available via e-mail request sent to:

railwaysafety@utrgv.edu

When finalized, they will also be posted at http://railwaysafety.utrgv.edu, in the Technology Transfer section.