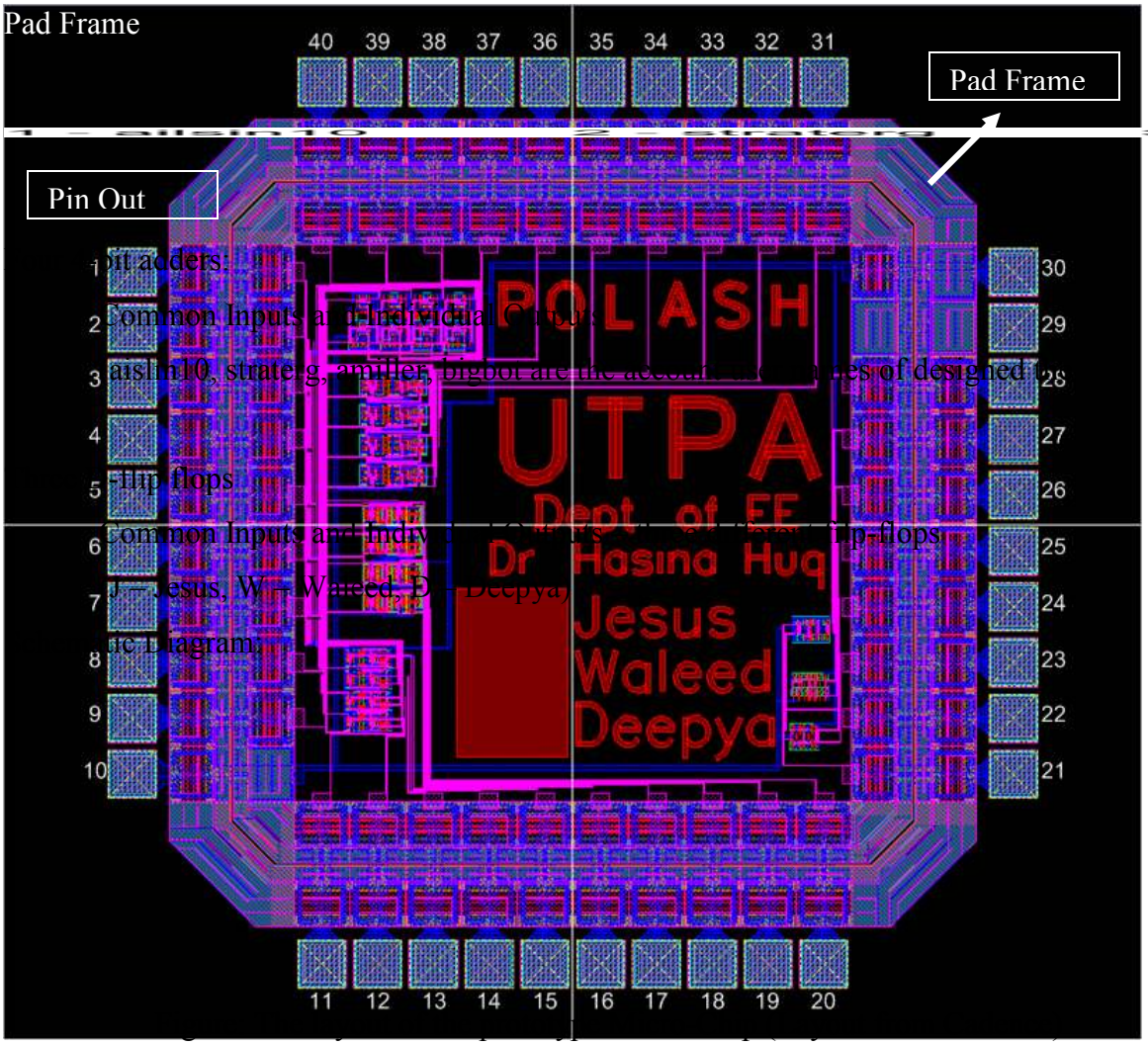
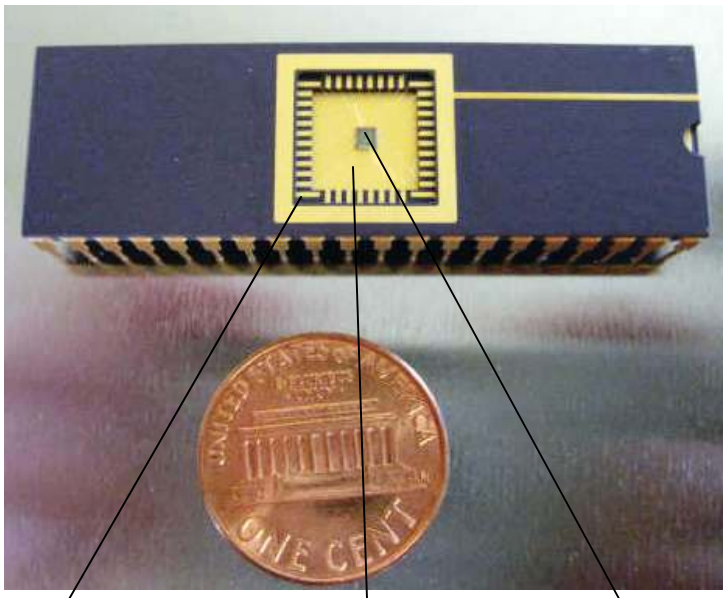
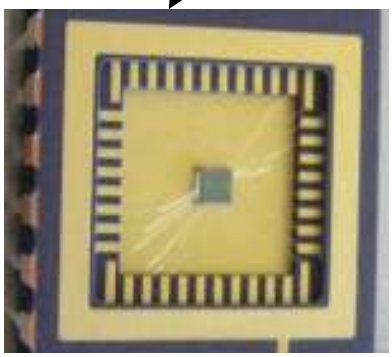


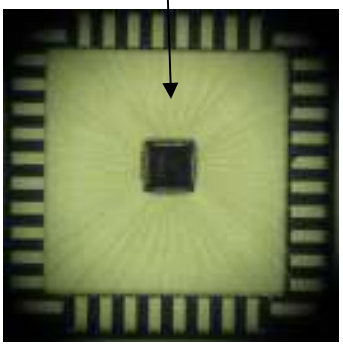
Integrated Circuit (IC) Design using CMOS technology; AMI 0.5 process



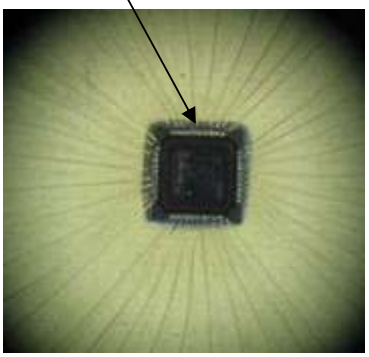
Fabricated IC by UTPA-EE students using MOSIS facilities (Packaged in DIP 40)



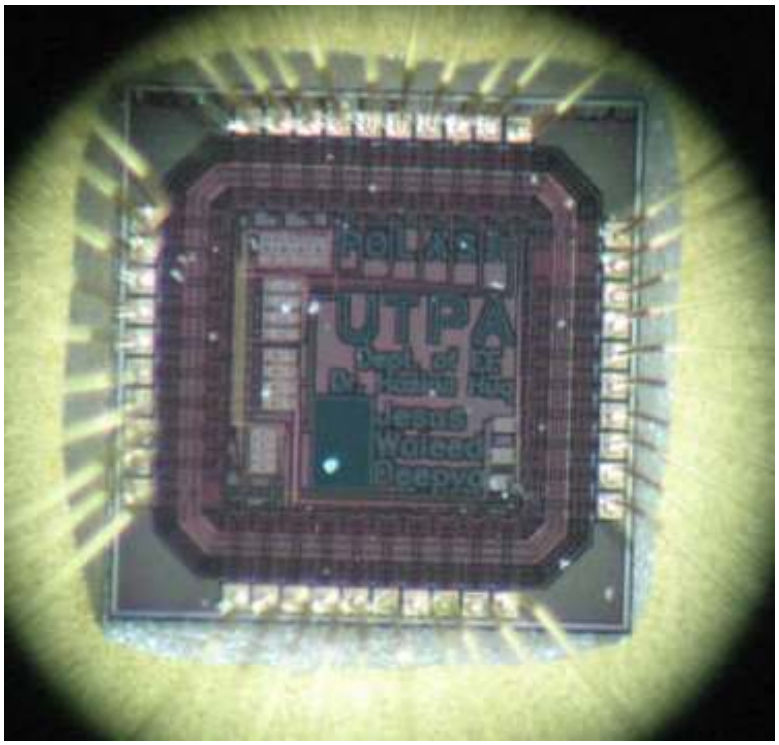
a) Pad frame



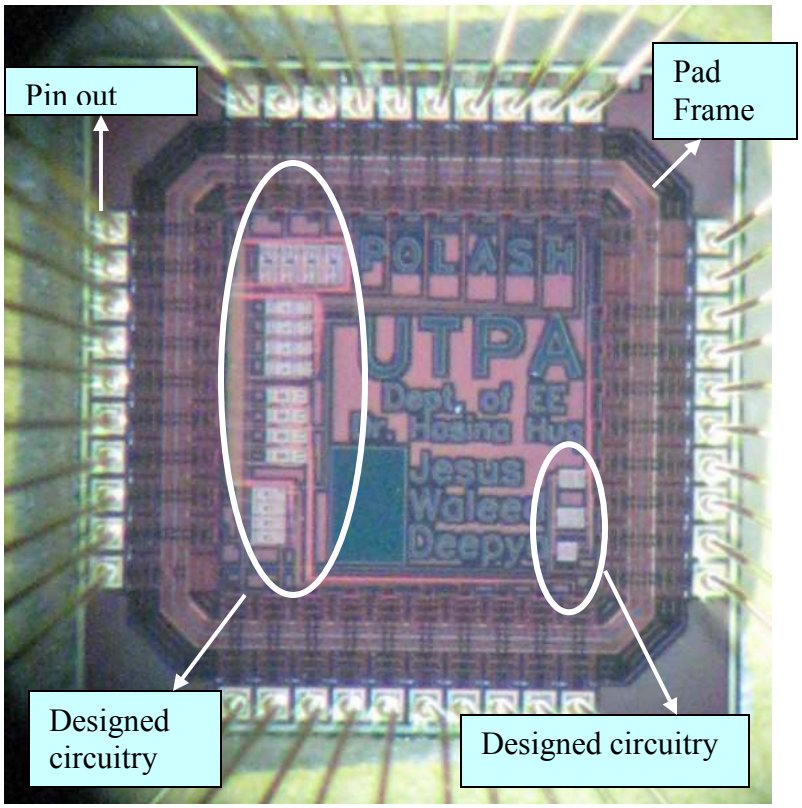
b) Wire Bonding Microscopic Image: Cavity Size 7874um X 7874um



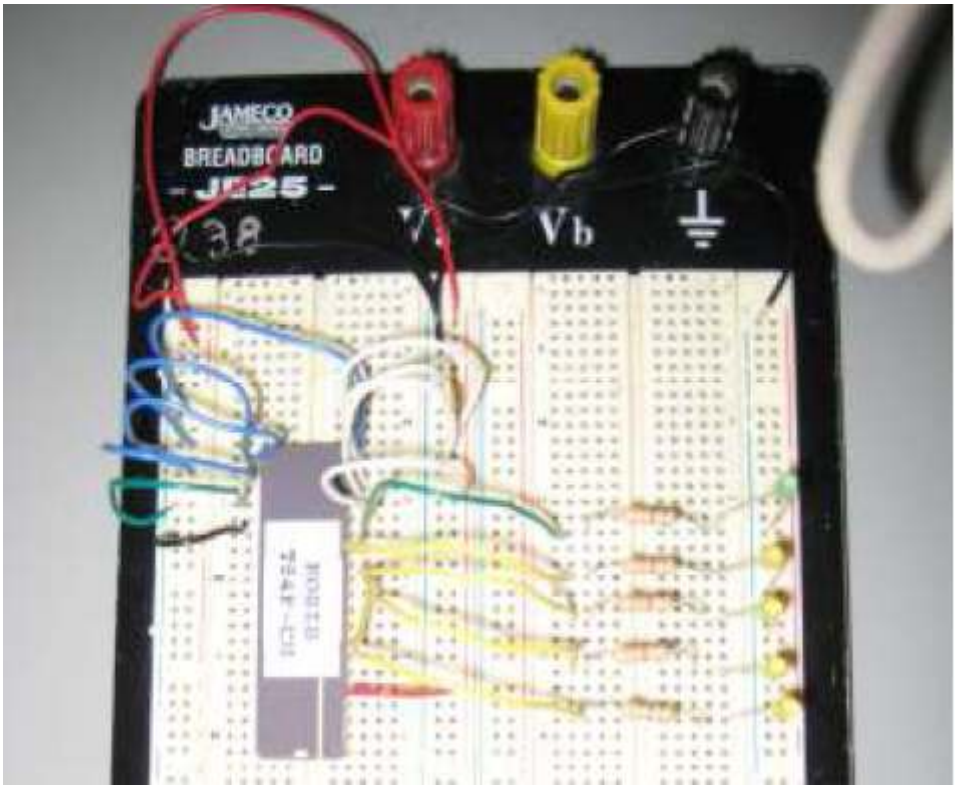
c) Designed IC on Si Wafer Microscopic Image: Die Size 1615umX1644 um



Designed IC on Si Wafer (Microscopic Image: Die Size 1615 um X 1644 um)



The prototype integrated circuit is developed using 0.5 micron standard CMOS process available through MOSIS.



Test board for the chip