The goal of this project is to design, simulate, fabricate and evaluate the integrated circuit (IC) design process by Computer-Aided Design (CAD) tool using Cadence software and IC design fabrication facility (MOSIS) services. In this project the graduate and undergraduate students created an integrated circuit which has more than 500 MOSFET transistors in a single pinhole size wafer (1615 um X 1644 um). Cadence provides front-to-back design tools and services for all aspects of semiconductor design. MOSIS provides access to fabrication of prototype and low-volume production quantities of the designed integrated circuits. The digital designs IC of our choice are the four bit full adder; an essential part of ALU (Arithmetic Logical Unit) and clocked D flip-flop; an essential component in most sequential circuits.

The designed D flip-flop (DFF) is used as a storing element to maintain only one value (0 or 1) every clock cycle assuring functional, observable and stable design output. The operating frequency range of the DFF is in MHz range (upto ~14 MHz) with a load 0 to 15 pf.

The designed adder can add up to four binary numbers. Each pair of bits in design can produce an output carry, it is also able to recognize and include a carry from the next lower order of magnitude.

The D flip-flops and the four bit full adder have been tested for functionality and performance and result comparison are conducted between both extracted results from simulation and experiment.

This project is the first IC design fabrication done by the Electrical Engineering students at UTPA. This project formed the foundation to future designs fabrication with much more complexity and creativity (System on a Chip). The students will benefit greatly in dealing with the industry of semiconductor devices and learning how to convert their design ideas into actual chip that can be experimentally tested to compare the experimental with the simulated data.