Fabrication of Enhancement Mode n-MOSFET by Physical Vapor Deposition Using Sputtering System and Study of Its I-V Characteristics

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ABSTRACT

In this work, we fabricated n-MOSFET samples using Physical Vapor Deposition (PVD) technique and studied their current-voltage (I-V) characteristics by software simulation and physical experimentation. Industrially, MOSFET is manufactured using Chemical Vapor Deposition (CVD) or Ion implantation and Oxidation process, which is different than the Physical Vapor Deposition (PVD) method we used to fabricate our MOSFET samples. An optimum combination of pressure and power was found out by thorough study to grow the epitaxial layers in the sputtering system; otherwise, the deposited samples might have shown excessive surface roughness and therefore, more internal resistance. The drain to source current (I_{ds}) of industrially manufactured MOSFETs in usually from 10^{-6}A (μA) to 10^{-3}A (mA) range. Our fabricated n-MOSFET samples showed a drain to source current (I_{ds}) of 4-7 μA when 5v was applied both as gate to substrate voltage (V_{GB}) and drain to source voltage (V_{DS}). Channel lengths of industrially manufactured MOSFETs vary from nm to μm range depending on the purpose. Our fabricated MOSFET samples, however, have bigger channel lengths but no bigger than 7mm. The overall dimensions of the fabricated MOSFET samples are also much bigger than the industrially manufactured models. Our fabricated n-MOSFET can be used as pressure sensor by connecting the gate metal contact layer with a piezoelectric material that can produce voltage by exerting pressure.

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Introduction

The **Metal Oxide Semiconductor Field Effect Transistor** (**MOSFET**) is the basic building block of modern electronics. It is considered the "workhorse" of the electronics industry. Industrially, n-wells and silicon oxide layer under the gate are fabricated by CVD/Ion implantation and oxidation processes, respectively.

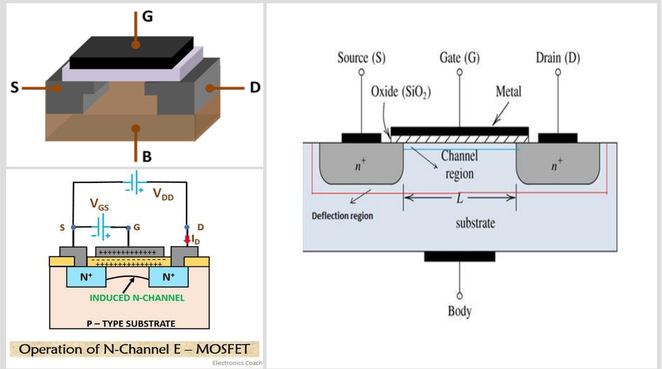
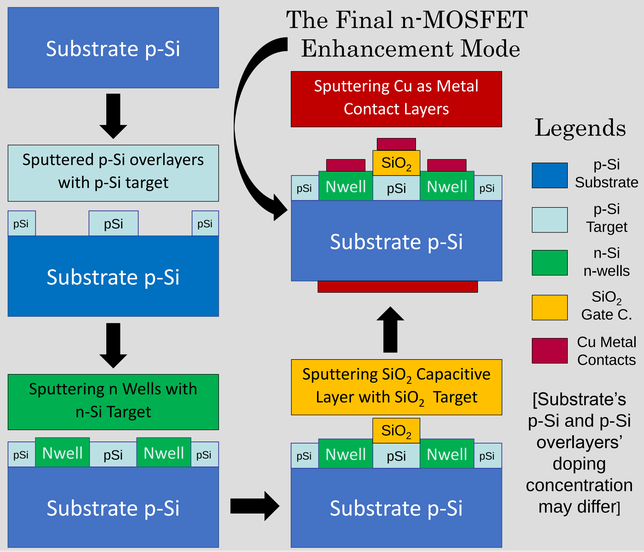


Figure: (1) MOSFET diagram and operation of enhancement mode n-MOS (left). (2) Cross-sectional image of n-MOS (right).

Here, sputtering system lab in UTRGV, we tried to fabricate enhancement mode n-MOSFET using PVD technique. MOSFET in enhancement mode works such way that- when there is no voltage across the gate terminal, then the device does not conduct. When there is the maximum voltage across the gate terminal, then the device shows enhanced conductivity.

Proposed Growing Technique



Methodology

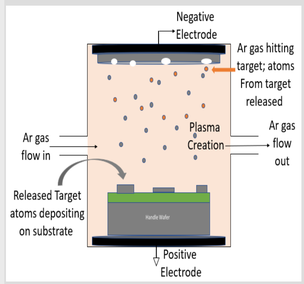


Figure: Sputtering System

RF Sputtering is used to sputter p-Si overlayers, n-Wells, SiO_2 and gate oxide layer over p-Si substrate. Cu contact was deposited using DC sputtering. Choice of sputtering recipe- pressure, power and time- is important because sputtering rate, layer thickness and surface morphology depend on these parameters.

Choice of Sputtering Parameters

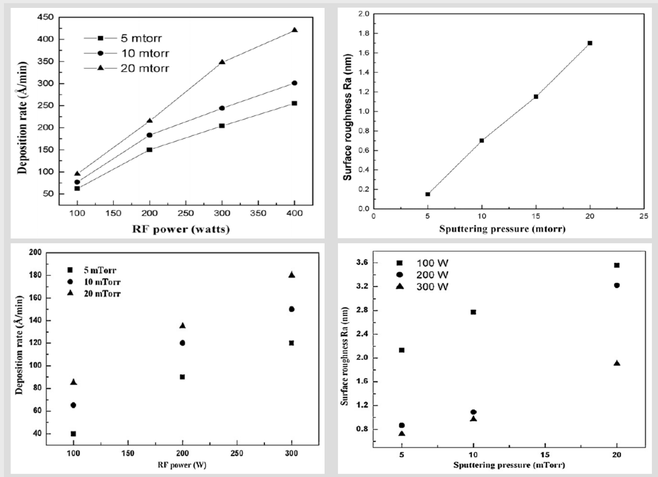


Figure: (1) Si deposition rate vs RF power and pressure (top left) [1]. (2) Si Surface roughness vs pressure (top right) [2]. (3) SiO_2 deposition rate vs RF power and pressure (bottom left) [3]. (4) SiO_2 surface roughness vs pressure & RF power [4].

p-Si, n-Si and SiO_2 Sputtering Recipe:

Parameters ⇨ / Materials ⇩	RF Power	Pressure	Ar Gas Flow Rate	Coating Time
p-Si(overlayers)	200 W	15mTorr	15sccm	10h
n-Si(N-wells)	200 W	15mTorr	15sccm	13h
SiO_2(ox. layer)	200 W	15mTorr	15sccm	8h

Sample Images

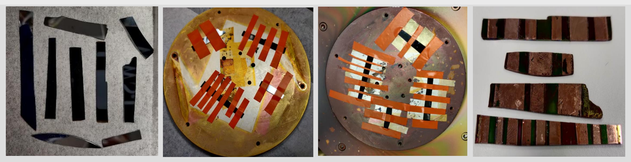


Figure: (1) Si sample substrate. (2) p-Si overlayers deposition and channel length. (3) n-well deposition and length. (4) Final n-MOSFET samples with Cu contact layers .

I-V Characteristics

$$I_D = \frac{1}{2} k_n \frac{W}{L} [(V_{GS} - V_T) V_{DS} - \frac{1}{2} V_{DS}^2]$$
When $[V_{DS} < V_{GS} - V_T]$
$$I_D = \frac{1}{2} k_n \frac{W}{L} (V_{GS} - V_T)^2$$
When $[V_{DS} \geq V_{GS} - V_T]$

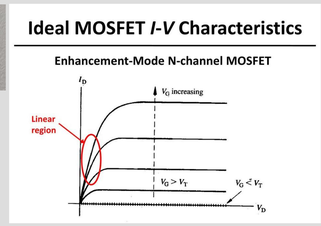
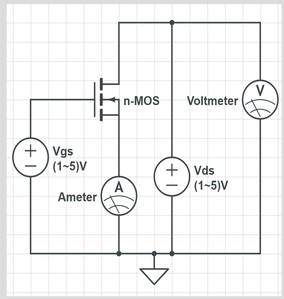


Figure: (1) Sample to study I-V characteristics (top left). (2) Ideal enhancement mode n-MOSFET I-V characteristics & equations



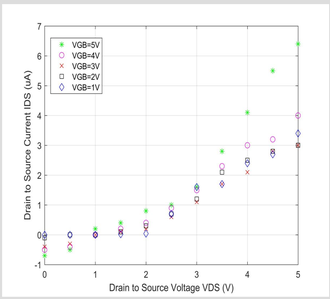


Figure: Circuit Schematics for figuring out n-MOS I-V characteristics (Left). Derived I-V characteristics of sample MOSFET (Right).

Discussion

1. We found similarities in I-V characteristics of Our enhancement type n-MOS sample with that of the ideal n-MOS.

2. Theoretically, if the pressure of deposition was lowered, the surface of the n-MOS would be smoother, henceforth, the resistance would be lower resulting is greater drain current.

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References

[1] P. Pal and S. Chandra, "RF sputtered silicon for MEMS", Journal of Micromechanics and Microengineering, 15 (2005) 1536–1546, doi:10.1088/0960-1317/15/8/023.

[2] V. Bhatt and S. Chandra, "Silicon dioxide films by RF sputtering for microelectronic and MEMS applications", Journal of Micromechanics and Microengineering, 17 (2007) 1066–1077, doi:10.1088/0960-1317/17/5/029.